# ADM-XA210
# User Manual

**Document Revision: 1.0**
**Mar 4, 2025**

| | Head Office | US Office |
|---|---|---|
| Address: | Suite L4A, 160 Dundee Street,<br>Edinburgh, EH11 1DQ, UK | 10822 West Toller Drive, Suite 250<br>Littleton, CO 80127 |
| Telephone: | +44 131 558 2600 | (303) 954 8768 |
| Fax: | +44 131 558 2700 | (866) 820 9956 - toll free |
| email: | sales@alpha-data.com | sales@alpha-data.com |
| website: | http://www.alpha-data.com | http://www.alpha-data.com |

# Table Of Contents

# List of Tables



# List of Figures

Page Intentionally left blank

# 1 Introduction

The ADM-XA210 is a high-performance XMC for applications using the Versal from AMD.

The ADM-XA210 is available in air-cooled and conduction-cooled configurations. View the Ordering Info tab at ADM-XA210 Product Page on www.alpha-data.com.

## 1.1 Key Features

**Key Features**

- Single-width XMC, compliant to VITA Standard 42.0, 42.3 and 42.10d12
- Support for VM1802 and VC1802 devices in VSVD1760 packages
- Voltage and temperature monitoring,
- Air-cooled and conduction-cooled configurations,
- Micro USB system platform manager with voltage and temperature measurements
- Processing System (PS) Block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - Removable microSD Flash memory
  - 8-bit wide Quad SPI Flash memory (2Gb)
  - 2 USB 2.0 ports to the rear P4 connector
  - 1 Gigabit Ethernet interfaces to the rear P4 connector
  - 1 CAN bus interface to rear P4 connector
  - 1 serial COM port interface to the rear P4 connector (configurable as either RS-232 or RS-422/485)
  - 4 single-ended PS GPIO pins to the P4 connector
- Programmable Logic (PL) block consisting of:
  - Standard XRM2 IO Interface to FPGA
  - 8 GTY links to the P5 connector, capable of 32Gbps
  - 8 GTY links to the P6 connector, capable of 32Gbps
  - 4 banks of 32-bit wide LPDDR4-4266 SDRAM (8GB total)
  - 1 serial COM port interface to the rear P4 connector (configurable as either RS-232 or RS-422/485)
  - 38 single-ended GPIO pins to the P6 connector

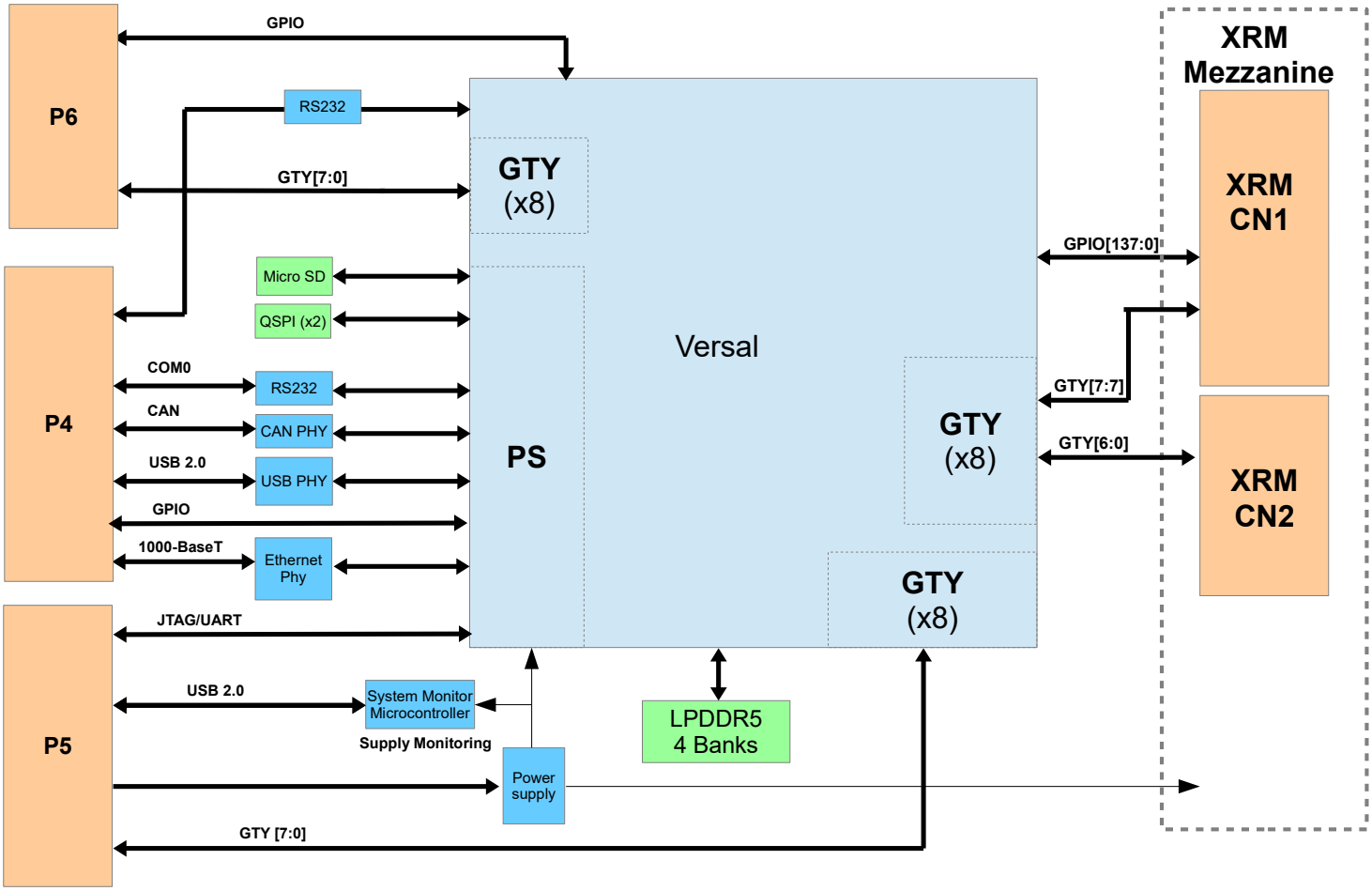



**Figure 1 : ADM-XA210 Block Diagram**

## 1.2 References & Specifications

| | |
|---|---|
| ANSI/VITA 42.0 | *XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3 |
| ANSI/VITA 42.2 | *XMC Serial RapidIO Protocol Layer Standard*, Feb 2006, VITA, ISBN 1-885731-41-8 |
| ANSI/VITA 42.3 | *XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4 |
| ANSI/VITA 46.9 | *PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9 |
| ANSI/IEEE 1386-2001 | *IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5 |
| ANSI/IEEE 1386.1-2001 | *IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7 |
| ANSI/VITA 20-2001 (R2005) | *conduction-cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4 |

**Table 1 : References**

# 2 Installation

## 2.1 Hardware Installation

### 2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

### 2.1.2 Motherboard / Carrier Requirements

The ADM-XA210 is a single-width XMC.3 mezzanine card equipped with P6 and P4 connectors. The motherboard or carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

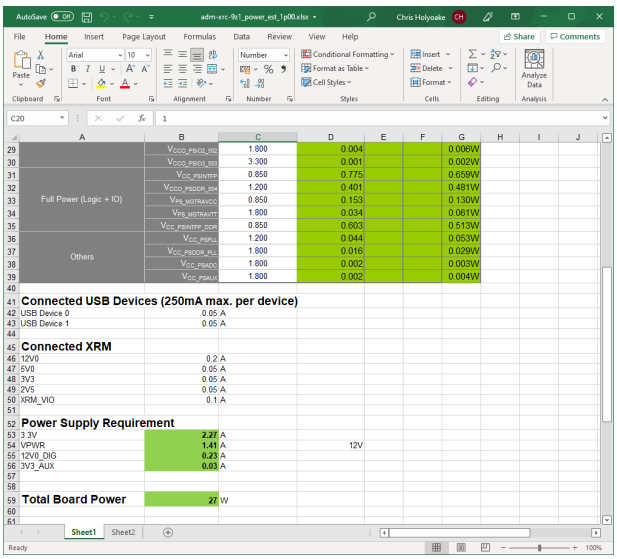
The Secondary XMC connector P6 has a pinout compatible with various XMC-to-VPX signal maps as defined by VITA 46.9. Before installation, refer to the pinout details in this user guide and those provided by the carrier manufacturer. Assistance can be provided by Alpha Data.

**IMPORTANT**
Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) standard. In particular, USB VCC must not be applied on this connector.

The ADM-XA210 is compatible with either 5V or 12V on the "VPWR" power rail.

### 2.1.3 Cooling Requirements

The power dissipation of the board is highly dependent on the FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with AMD power estimation tools to determine the exact current requirements for each power rail.



| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | $V_{CCO\_PSIO3\_503}$ | 1.800 | 0.004 | | | 0.006W |
| | $V_{CCO\_PSIO1\_503}$ | 3.300 | 0.001 | | | 0.002W |
| Full Power (Logic + IO) | $V_{CC\_PSINTFP}$ | 0.850 | 0.775 | | | 0.659W |
| | $V_{CCO\_PSDDR\_504}$ | 1.200 | 0.401 | | | 0.481W |
| | $V_{PS\_MGTRAVCC}$ | 0.850 | 0.153 | | | 0.130W |
| | $V_{PS\_MGTRAVTT}$ | 1.800 | 0.034 | | | 0.061W |
| | $V_{CC\_PSINTFP\_DDR}$ | 0.850 | 0.603 | | | 0.513W |
| Others | $V_{CC\_PSFLL}$ | 1.200 | 0.044 | | | 0.053W |
| | $V_{CC\_PSDDR\_PLL}$ | 1.800 | 0.016 | | | 0.029W |
| | $V_{CC\_PSADC}$ | 1.800 | 0.002 | | | 0.003W |
| | $V_{CC\_PSAUX}$ | 1.800 | 0.002 | | | 0.004W |

| | | | |
|---|---|---|---|
| **Connected USB Devices (250mA max. per device)** | | | |
| USB Device 0 | 0.05 | A | |
| USB Device 1 | 0.05 | A | |
| **Connected XRM** | | | |
| 12V0 | 0.2 | A | |
| 5V0 | 0.05 | A | |
| 3V3 | 0.05 | A | |
| 2V5 | 0.05 | A | |
| XRM_VIO | 0.1 | A | |
| **Power Supply Requirement** | | | |
| 3.3V | 2.27 | A | |
| VPWR | 1.41 | A | 12V |
| 12V0_DIG | 0.23 | A | |
| 3V3_AUX | 0.03 | A | |
| **Total Board Power** | 27 | W | |

**Figure 2 : Alpha Data Power Estimator Spreadsheet**

The board is supplied with a passive air-cooled or conduction-cooled heat-sink according to the order number specified at time of purchase. It is the user's responsibility to ensure sufficient airflow for air-cooled applications and metalwork for conduction-cooled applications.

The board features a system monitor that measures the board and FPGA temperatures. It also includes a self-protection mechanism that clears the FPGA configuration if an over-temperature condition is detected.

See Section 5.9 for further details.

# 3 Mechanical

| Parameter | Condition | Value |
|---|---|---|
| Length | AC1 | 149.0mm |
| Length | CC1 | 143.75mm |
| Width | - | 74.0mm |
| Weight | No Heatsink | 74.0mm |
| Weight | AC Assembly | TBD g |
| Weight | CC Assembly | TBD g |

**Table 2 : Mechanical Info**

# 4 Example Design

An FPGA and CPIS ARM/Linux example design is available, contact support@alpha-data.com for access. It provides an interactive interface or command line interface to control the board features.

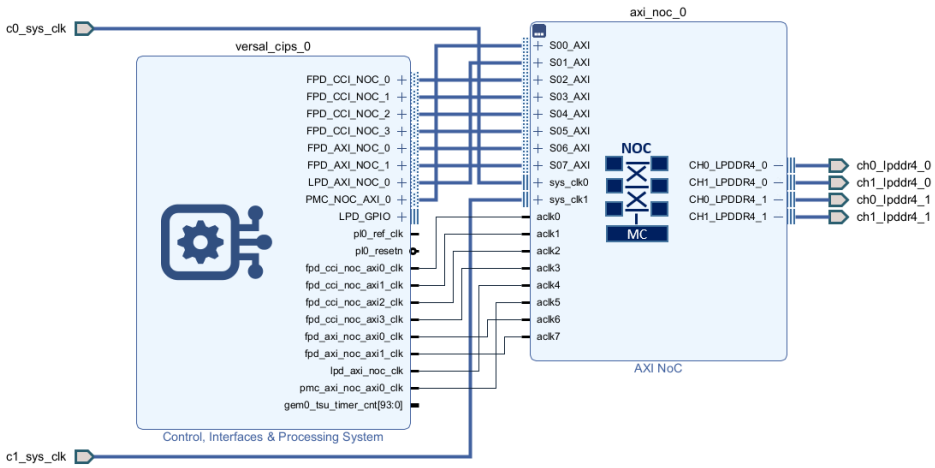



**Figure 3 : ADM-XRC-9R1B Vivado Example Design**

# 5 Functional Description

## 5.1 Overview

### 5.1.1 Switch Definitions

There are two sets of eight DIP switches (16 switches in total) placed on the rear of the board. Some switch states can be controlled using the FPGA or the AVR system monitor. These signals are shown in the corresponding table. Signals controllable by the system monitor can be controlled using the AVR2Util utility (See Section 5.9.3 for information on using AVR2Util).

The default switch states for SD card boot mode are SW1[8:1]:00001100 and SW2[4:1]:0000. SW1-6 can either be ON or OFF depending on whether the card is used with a carrier with a JTAG connection to the XMC site.

**Note:**
*The factory configuration* switch (SW2-5) must be in the OFF position for normal operation.

| Switch Ref. | Function | Override | ON State | Off State |
|---|---|---|---|---|
| SW1-1 | BootMode 0 | Yes | See Table 12 | |
| SW1-2 | BootMode 1 | Yes | See Table 12 | |
| SW1-3 | BootMode 2 | Yes | See Table 12 | |
| SW1-4 | MRSTO Enable | No | MRSTO FPGA pin W9 is isolated from XMC connector | MRSTO FPGA pin W9 is connected to XMC connector |
| SW1-5 | *Factory Configuration* | No | - | Normal Operation |
| SW1-6 | XMC JTAG Enable | No | XMC JTAG interface enabled | XMC JTAG interface disabled |
| SW1-7 | XMC PCIE reset enable | No | XMC PCIE reset connected to PS | XMC PCIE reset disconnected to PS |
| SW1-8 | PS Reset | Yes | PS is held in reset | Normal Operation |

**Table 3 : SW1 Switch Definitions**

| Switch Ref. | Function | ON State | Off State |
|---|---|---|---|
| SW2-1 | UART0 RS485 Enable | COM0 RS485 Enabled | COM0 RS485 Disabled |
| SW2-2 | UART1 RS485 Enable | COM1 RS485 Enabled | COM1 RS485 Disabled |
| SW2-3 | USB UART Enable | USB to UART converter Enabled | USB to UART converter Disabled |
| SW2-4 | User Switch | FPGA pin R6 High | FPGA pin R6 Low |

**Table 4 : SW2 Switch Definitions**

Pins controlled by the system monitor are non-volatile, allowing the Boot Mode and other configurations to be retained between power cycles [1].

*[1]: If the boot mode is overridden by the system monitor, then 3V3_AUX must be applied before power-up in order to ensure the pins are configured before the boot mode pins are sampled. If 3V3_AUX is powered up at the same time as the main power, an incorrect boot mode may be selected.*

### 5.1.2 LED Definitions

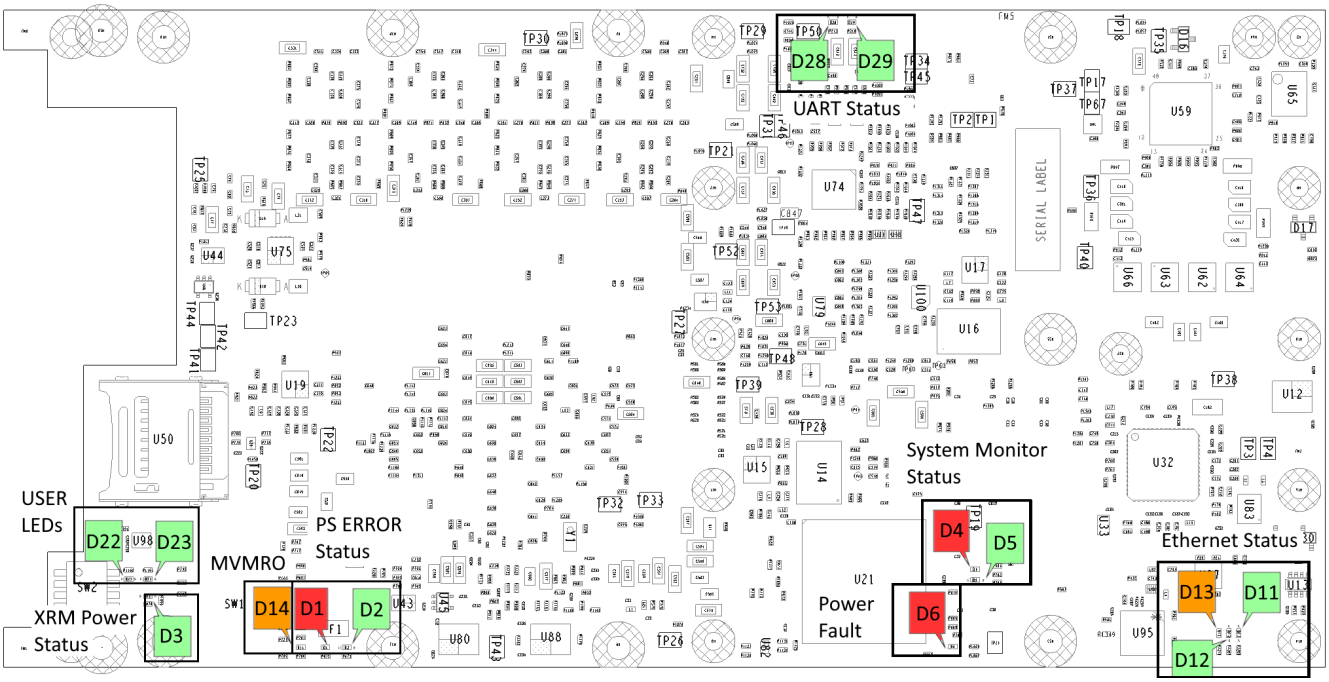



**Figure 4 : LED Locations**

| Comp. Ref. | Function | ON State | OFF State |
|---|---|---|---|
| D1 (Red) | PS ERROR | PS ERROR | PS OK |
| D2 (Green) | PS_DONE | FPGA Configured | FPGA Not configured |
| D22 (Green) | USER LED 0 | FPGA Pin Y13 High | FPGA Pin Y13 Low |
| D23 (Green) | USER LED 1 | FPGA Pin Y13 High | FPGA Pin Y13 Low |
| D3 (Green) | XRM Power OK | XRM Powered Up | XRM Not Powered |
| D5 (Green) | Status 0 | See Status LED Definitions | |
| D4 (Red) | Status 1 | See Status LED Definitions | |
| D6 (Red) | Power Fault | Power supply error | Power supplies good |
| D28 (Green) | USB UART Data activity | PS RX Data activity | No PS RX Data Activity |
| D29 (Green) | USB UART Data activity | PS TX Data activity | No PS TX Data Activity |
| D11 (Green) | Ethernet Activity | See Ethernet Status LEDs | |
| D12 (Green) | Ethernet Activity | See Ethernet Status LEDs | |
| D13 (Amber) | Ethernet Activity | See Ethernet Status LEDs | |
| D14 (Amber) | MVMRO Status | Memory not write protected | Memory write protected |

**Table 5 : SW2 Switch Definitions**

## 5.2 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two Samtec connectors, CN1 and CN2.

### 5.2.1 XRM Connector CN1

Connector CN1 is for general-purpose signals, power and module control. It is a 180-way Samtec connector with 3 fields.

The part fitted to the ADM-XA210 is the Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is provided in XRM Connector CN1, Field 1 to XRM Connector CN1, Field 3.

### 5.2.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the ADM-XA210 is the Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is provided in XRM Connector CN2.

### 5.2.3 XRM I/F - GPIO

The general-purpose IO (GPIO) signals are connected in 4 groups to the FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs, and any can be used in single-ended modes.

To allow fast data transfer, all GPIO signals within a group are delay-matched to within 100 ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, which can be either 1.8V, 1.5V or 1.2V. The required voltage is stored within the platform management PROM on the XRM.

| Group | FPGA Bank | Name | Function |
|---|---|---|---|
| Group A | 16-17 | XRM_DA (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DA_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SA (1:0) | 2 single-ended GPIO |
| Group B | 15-16 | XRM_DB (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DB_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SB (1:0) | 2 single-ended GPIO |
| Group C | 15 | XRM_DC (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DC_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SC (1:0) | 2 single-ended GPIO |
| Group D | 17 | XRM_DD (15:0) | 16 diff. Pairs / 32 single-ended |
| | | XRM_DD_CC (16) | Regional Clock / GPIO pair / 2 single-ended |
| | | SD (3:0) | 4 single-ended GPIO |

**Table 6 : XRM GPIO Groups**

### 5.2.4 XRM I/F - High-Speed Serial Links

Eight MGT links are routed between the FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

### 5.2.5 XRM IO Voltage Override

Each XRM is built with an I2C EEPROM that contains vital product information (VPD) such as part number, serial number, operating voltage, and product-specific information. For designing custom XRMs, contact Alpha Data for details on duplicating this VPD data.

Alternatively, FORCE2V5_L can be driven low to select 1.8V for the front I/O voltage. Note that FORCE2V5_L is a signal name from a historical design, and the operating voltage will not be 2.5V but rather 1.8V if this mode is used.

## 5.3 XMC Platform Interface

### 5.3.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC base specification.

### 5.3.2 MBIST#

Built-In Self Test: This output signal is connected to FPGA pin AW24. It is not driven by default, and has a 4.75kOhm pull-up resistor.

### 5.3.3 MVMRO

XMC Write Prohibit: This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D2.

The MVMRO signal has a 100KΩ pull-up resistor fitted by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the FPGA at pin AV27.

### 5.3.4 MRSTI#

XMC Reset In: This signal is an active-low input from the carrier. This signal connected to the PS at pin L30. This signal can also drive the PS power-on-reset pin, depending on SW1-7

A buffered version of MRSTI# is also connected to the FPGA at pin Y10.

### 5.3.5 MRSTO#

XMC Reset Out: This optional output signal is driven from the FPGA pin V12. This signal is passed through a tristate buffer controlled by SW1-5 to optionally isolate the FPGA from MRSTO. There are pull-ups on both sides of the buffer so that MRSTO is always de-asserted unless the FPGA actively drives it low.

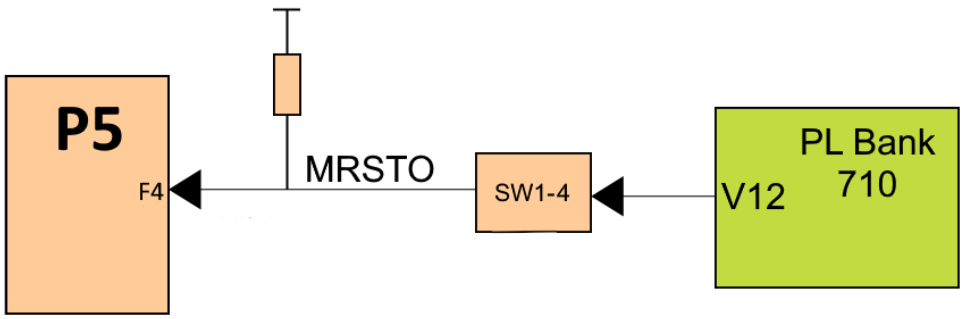



**Figure 5 : MRSTO Circuit**

### 5.3.6 MPRESENT#

Module Present: This output signal is connected directly to GND.

# 5.4 JTAG Interface

## 5.4.1 On-board JTAG Interface

A JTAG boundary scan chain is connected to header U42. This allows the connection of an AMD JTAG cable for FPGA debug using the AMD tools. The ADM-XA210 comes with an adaptor board that attach to this connector, providing access to a standard 14-pin JTAG header that is compatible with the AMD Platform II JTAG box. The adaptor board connects through holes at the rear of the PCBm enabling JTAG accessed while the board is mounted to a carrier.

The JTAG Header location is shown in JTAG Header U42:

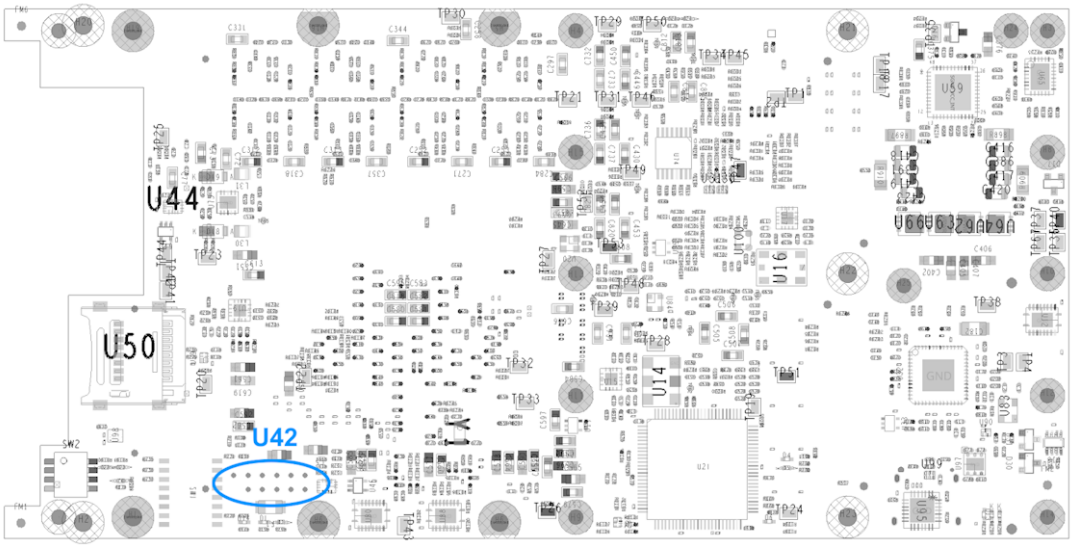



**Figure 6 : JTAG Header U42**

The scan chain is shown in JTAG Boundary Scan Chain:

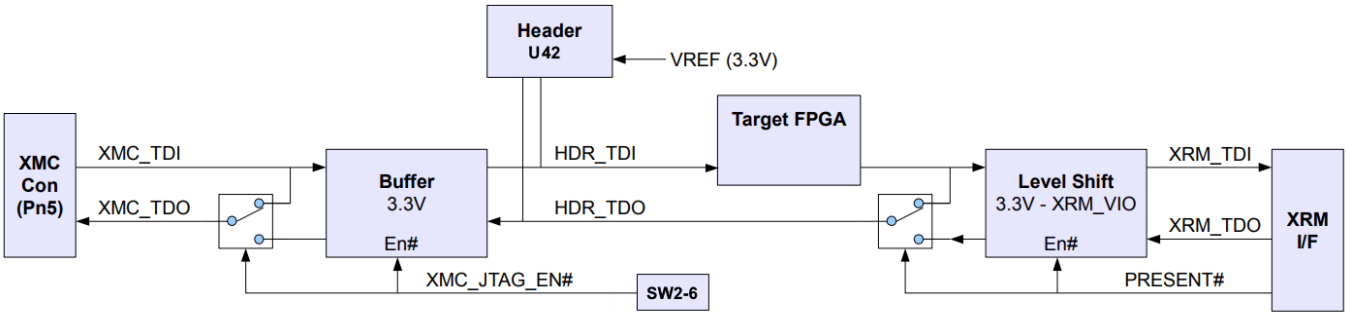



**Figure 7 : JTAG Boundary Scan Chain**

SW2-6 controls whether the JTAG interface connects to U42, or to the P5 XMC connector. This setting can also be controlled using the on-board AVR system monitor, either using the micro USB interface or from the PS using the on-board serial interface between the PS and the AVR. If the boundary scan chain is connected to the interface at the XMC connector (SW1-6 is ON), header U42 is disconnected.

### 5.4.2 XMC JTAG Interface

When the JTAG interface on the XMC connector is unused, XMC_TDI connected directly to XMC_TDO to loop back the JTAG chain.

The XMC_JTAG interface can be connected to the on-board JTAG interface (through level-translators) by switching SW1-5 ON. See Switch Definitions.

### 5.4.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The VCC supply provided on J2 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 375mA.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM interface use the adjustable voltage XRM_VIO.

## 5.5 Clocks

The ADM-XA210 provides a wide variety of clocking options, using some fixed oscillators and a user-programmable clock generator. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

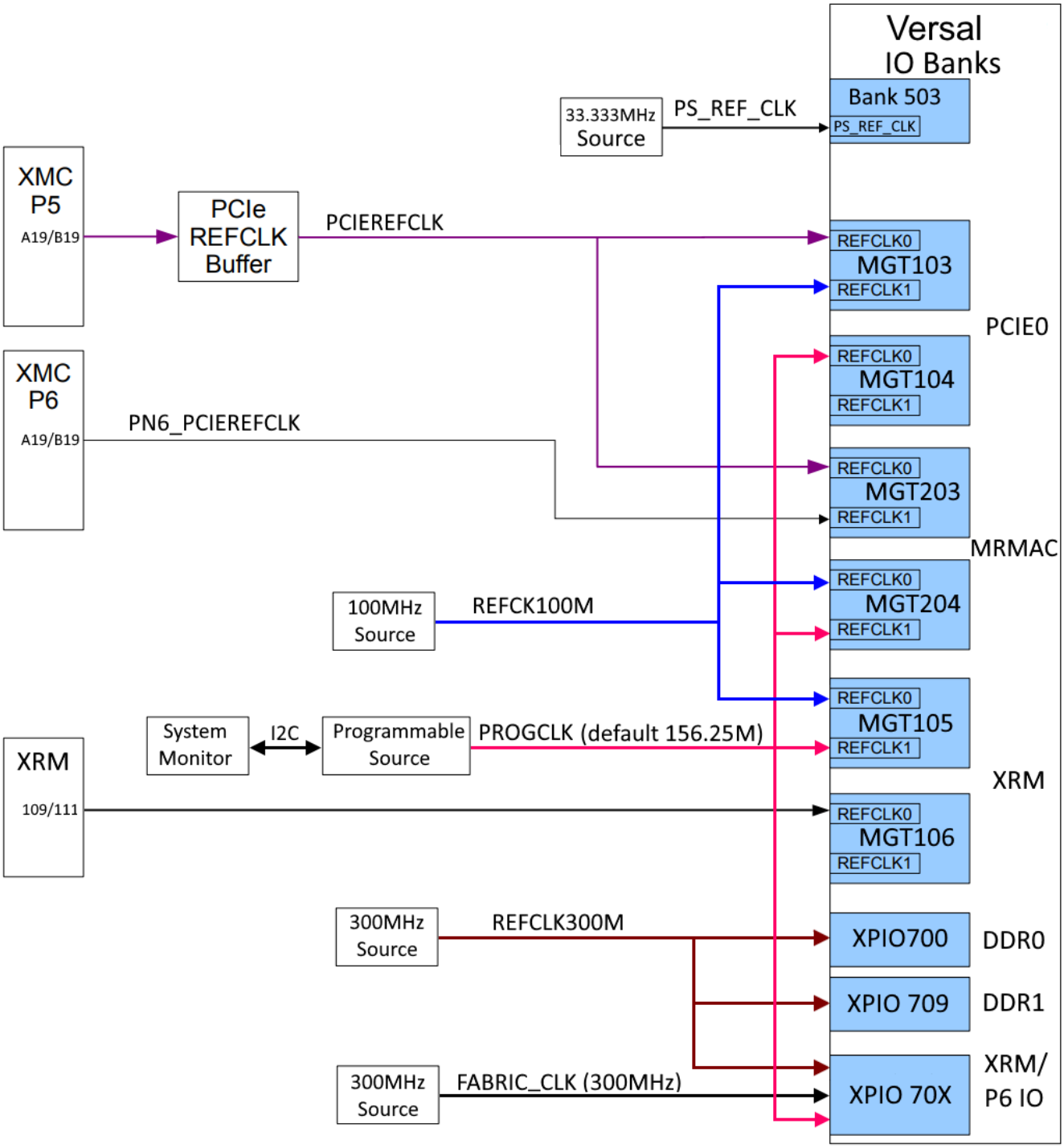



**Figure 8 : Board Clock Diagram**

### 5.5.1 300 MHz Reference Clocks (MEM_CLK and FABRIC_CLK)

The fixed 300 MHz reference clocks, MEM_CLK and FABRIC_CLK, are differential LVDS signals.

MEM_CLK0 and MEM_CLK1 are used as the input clocks for the LPDDR4 SDRAM interfaces.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

| Signal | Frequency | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|
| MEM_CLK0 | 300 MHz | LVDS | AF36 | AF37 |
| MEM_CLK1 | 300 MHz | LVDS | AR28 | AT29 |
| FABRIC_CLK | 300 MHz | LVDS | AC7 | AC6 |

**Table 7 : 300 MHz Connections**

### 5.5.2 PCIe Reference Clocks (PCIEREFCLK)

The 100 MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector P5 at pins A19 and B19. This clock is buffered into two PCIe Express reference clocks that are forwarded to the GTY transceivers.

| Signal | Frequency | FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| PCIEREFCLK0 | 100 MHz | GTY_REFCLKP0_103 | LVDS | AB34 | AB35 |
| PCIEREFCLK1 | 100 MHz | GTY_REFCLKP1_203 | LVDS | B17 | A17 |

**Table 8 : PCIEREFCLK Connections**

### 5.5.3 PN6 Reference Clock (PN6_REFCLK)

The reference clock PN6_REFCLK is a differential clock provided by a carrier card through the Secondary XMC connector P6 at pins A19 and B19. This board connects this pair to an MGT clock input.

| Signal | Frequency | FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| PN6_REFCLK | Carrier Defined | GTY_REFCLKP0_203 | LVDS | B15 | A15 |

**Table 9 : PN6_REFCLK Connections**

### 5.5.4 Programmable Clocks (PROGCLK 0-3)

There is one programmable clock source that is forwarded throughout the FPGA. This clock is programmable through the USB system monitor. PROGCLK[2:0] are generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments). PROGCLK[3:0] are all buffered copies of the same clock signal.

| Signal | Frequency | FPGA Input | IO Standard | "P" pin | "N" pin |
|---|---|---|---|---|---|
| PROGCLK0 | 5 - 312.5 MHz | GTY_REFCLKP0_104 | LVDS | W36 | W37 |
| PROGCLK1 | 5 - 312.5 MHz | GTY_REFCLKP0_204 | LVDS | D18 | C18 |
| PROGCLK2 | 5 - 312.5 MHz | GTY_REFCLKP1_105 | LVDS | N36 | N37 |
| PROGCLK3 | 5 - 312.5 MHz | PL Bank 708 | LVDS | AJ7 | AH6 |

**Table 10 : PROGCLK Connections**

### 5.5.5 Fixed Oscillators

There are five fixed oscillators on the board for the digital system. The USB and Ethernet reference clocks are used internally by the PHYs.

| Signal | Frequency | FPGA pin |
|---|---|---|
| PS Ref Clock | 33.3333MHz | AD28 |
| USB Ref Clock | 24MHz | - |
| USB Hub Ref Clock | 48MHz | - |
| Ethernet Ref Clock | 25MHz | - |

**Table 11 : Reference Clocks Connections**

# 5.6 PS Block

## 5.6.1 Boot Modes

| BootMode0 (SW2-1) | BootMode1 (SW2-2) | BootMode2 (SW2-3) | Boot Mode |
|---|---|---|---|
| ON | ON | ON | JTAG |
| ON | ON | OFF | Quad SPI |
| ON | OFF | OFF | SD Flash |
| - | - | - | Reserved |

**Table 12 : Boot Mode Selection**

## 5.6.2 Quad SPI Flash Memory

1 Gb Flash Memory (2x Micron MT25QU512AB) is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream.

The flash memory can only be accessed by the PS.

Utilities for erasing, programming and verification of the flash memory are available in Linux.

**Write Protect**

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED as shown in LED Locations.

## 5.6.3 MicroSD Flash Memory

A microSD card is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream. The SD Card can only be accessed by the PS.

### 5.6.4 Ethernet Interfaces

The **XA210** has one 1000BASE-T Ethernet interface at the rear connector P4.

The interface uses a Marvell 88E1512 PHY, connected to the PS via RGMII.

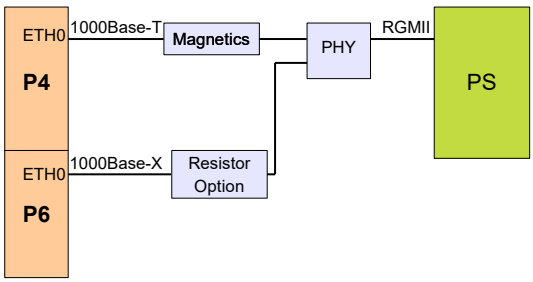



**Figure 9 : Ethernet Interface**

The interface has three status LEDs. The functions of these are shown in Table 13 below.

| Eth0 LED | Colour | Function |
|---|---|---|
| D11 | Green | On = Link up |
| D12 | Green | Unused |
| D13 | Amber | On = Link up |

**Table 13 : Ethernet Status LEDs**

### 5.6.5 Serial COM Ports

There is one PS COM port connected to the PMC connector P4, as shown in Serial COM Ports. The default speed of this COM port is 115.2k.

The COM ports use RS-232 by default but may be configured for RS-485, controlled by SW2-1 and SW2-2. When in RS-485 mode, the pinout of any external COM ports may not be standard.

The system monitor UART connects to both the PS and the PL, so the unused interface must be tri-stated to avoid IO pin conflicts.

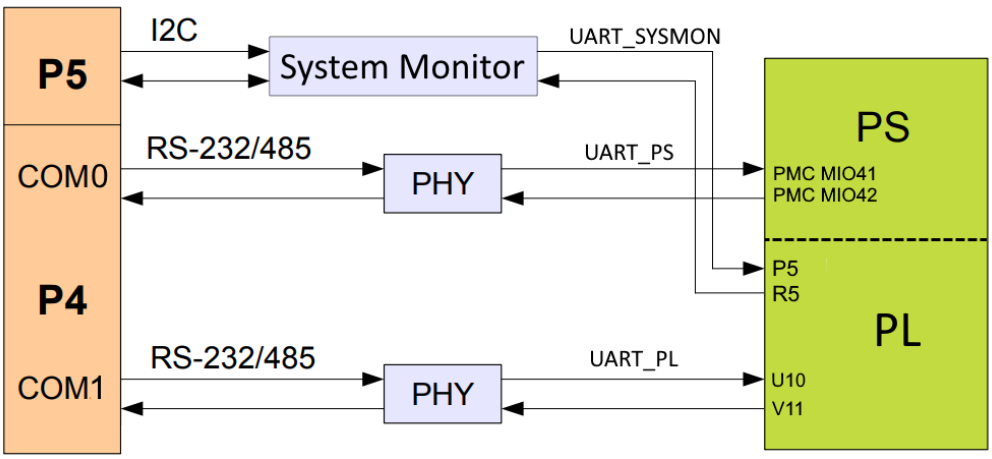



**Figure 10 : Serial COM Ports**

### 5.6.6 USB Interfaces

The ADM-XA210 has two external USB interfaces connected to the rear connector P4.

The PS is configured as the USB host for these external interfaces.

The on-board system monitor is accessible from the micro-USB connector.

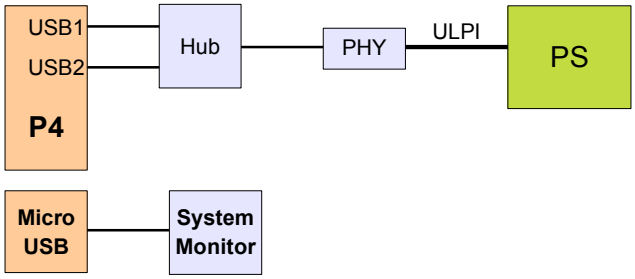



**Figure 11 : USB Interfaces**

### 5.6.7 PS GPIO

There are 4 single-ended GPIO pins from the PS to the P4 connector, which are compatible with 3.3V signalling such as TTL and CMOS. These GPIO pins are passed through a Texas Instruments TXS0108E level translator, capable of open-drain and push-pull level translation. The level translator is auto-direction-sensing. The level translator has a propagation delay of 5.7 ns max and a channel-to-channel skew (within a package) of 1 ns. It is suitable for rates up to ~50 Mb/s.

The PS GPIO are shown in GPIO Block Diagram.

# 5.7 PL Interfaces

## 5.7.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with its own power supply pins. The bank numbers, their voltage and function are shown in FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the constraint files of ADM-XA210 example designs.

| IO Banks | Voltage | Purpose |
|---|---|---|
| 503 | 3.3V | Configuration, JTAG, Boot Mode Select |
| 710, 711 | 1.5V | SE GPIO, Board Control |
| 67 | 1.8V | Diff. GPIO, Board Control |
| 706, 707, 708, 709 | Variable | XRM IO |
| 700, 701, 702 | 1.1V | PL LPDDR4 Bank 0 |
| 703, 704, 705 | 1.1V | PL LPDDR4 Bank 1 |

**Table 14 : FPGA IO Banks**

## 5.7.2 MGT Links

There are a total of 24 Multi-Gigabit Transceiver (MGT) links connected to the FPGA:

For MGT clocking see Board Clock Diagram:

The connections of these links are shown in MGT Links:

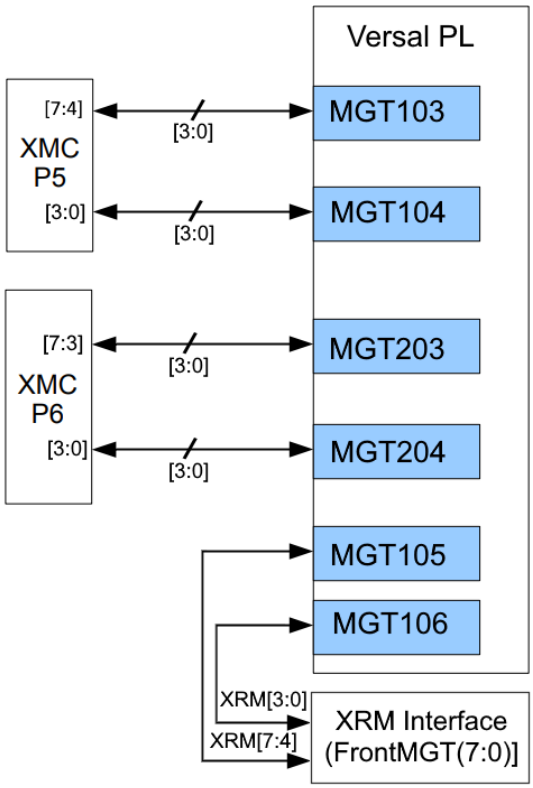



**Figure 12 : MGT Links**

### 5.7.3 PL GPIO

There are 38 single-ended GPIO pins from the FPGA to the P6 connector, which are compatible with 3.3V signalling such as TTL and CMOS. These GPIO pins are passed through a Texas Instruments TXS0108E level translator, capable of open-drain and push-pull level translation. The level translator is auto-direction-sensing. The level translator has a propagation delay of 5.7 ns max and a channel-to-channel skew (within a package) of 1 ns. It is suitable for rates up to ~50 Mb/s.

The P6 GPIO pin mapping is shown in Pn6 GPIO Pin Map, and P4 GPIO is shown in PMC Connector P4.

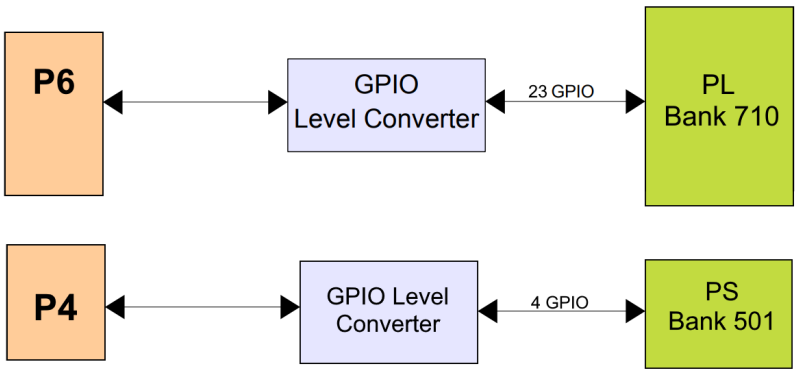



**Figure 13 : GPIO Block Diagram**

### 5.7.4 Memory Interfaces

The ADM-XA210 has two independent banks of LPDDR4 SDRAM. Each bank consists of two 32-bit wide memory devices, each device made up of two 16-bit channels, capable of running at up to 2133MHz (DDR-4266) . 16Gbit devices (Micron MT53E512M32D1ZW-046) are fitted as standard.

The memory banks are arranged for compatibility with the AMD NoC. PL DRAM Banks shows the component references and FPGA banks used. Full details of the interface, signalling standards and an FPGA design are provided in the ADM-XA210 example design.

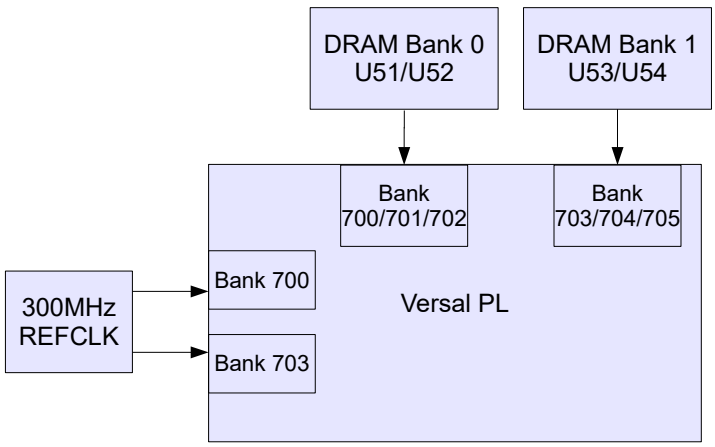



**Figure 14 : PL DRAM Banks**

# 5.8 Configuration

## 5.8.1 Power-Up Sequence

At power-up, the PS loads the first-stage bootloader from the memory interface selected by the Boot Mode select switches.

The first stage bootloader is responsible for configuring the FPGA and PS attached interfaces.

> **Note:**
> If an over-temperature alert is detected by the System Monitor, the FPGA is cleared by pulsing its PROG signal. See Automatic Temperature Monitoring.

# 5.9 System Monitoring

The ADM-XA210 has the ability to monitor temperature and voltage to maintain a check on the operation of the board. This monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically check line voltages and onboard temperatures and share the information with the PL.

See section Serial COM Ports for more details about the physical interface.

The following voltage rails and temperatures are monitored:

| **Monitor** | *Purpose* |
|---|---|
| VPWR | Board Input Supply (either 5.0V or 12.0V) |
| 12.0V | Board Input Supply |
| 5.0V | Internally generated 5V supply |
| 3.3V | Board Input Supply |
| 2.5V | Internally generated 2.5V supply |
| VCCINT | FPGA Core Supply (0.80V) |
| 0.8V | Internally generated 0.80V supply |
| 0.8V | Internally generated 0.80V supply |
| 0.88V | Internally generated 0.88V supply |
| 1.1V | Internally generated 1.1V supply |
| 1.5V | Internally generated 1.5V supply |
| 1.5V | Internally generated 1.5V supply |
| 1.2V | Internally generated 1.2V supply |
| XRM_VIO | Variable XRM IO supply |
| Temp0 | Microcontroller on-die temperature (unreliable, do not use) |
| Temp1 | Board temperature sensor on-die temperature |
| Temp2 | FPGA on-die temperature |

**Table 15 : Voltage and Temperature Monitors**

### 5.9.1 Automatic Temperature Monitoring

The onboard system monitor microcontroller contains pre-programmed temperature limits. These limits are shown in Temperature Limits:

| | Target FPGA | | Board | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| Commercial | 0 degC | +85 degC | 0 degC | +85 degC |
| Extended | 0 degC | +100 degC | 0 degC | +100 degC |
| Industrial | -40 degC | +100 degC | -40 degC | +100 degC |

**Table 16 : Temperature Limits**

**Important:**

If a temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by the Green LED (Target Configured or DONE) switching off and the two status LEDs showing a temperature fault indication. This condition is cleared with a power cycle.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang" as a result of communication errors.

An over-temperature shutdown will not occur until the system monitor reads 5 degC above the maximum limit for multiple samples in a row (i.e. +105 degC for Industrial boards). This is to compensate for potential errors in the temperature readings. There is no protection mechanism in place for minimum temperatures or the "Board" temperature sensor limits.

### 5.9.2 Microcontroller Status LEDs

LEDs D4 (Red) and D5 (Green) indicate the microcontroller status.

| **LEDs** | *Status* |
|---|---|
| Green | Running and no alarms |
| Green + Red | Standby (Powered off) |
| Flashing Green + Flashing Red (together) | Attention - critical alarm active |
| Flashing Green + Flashing Red (alternating) | Service Mode |
| Flashing Green + Red | Attention - alarm active |
| Red | Missing application firmware or invalid firmware |
| Flashing Red | FPGA configuration cleared to protect board |

**Table 17 : Status LED Definitions**

### 5.9.3 System Monitor Interfaces

There are two ways to communicate with the System Monitor to retrieve board status information on the ADM-XA210. One is through the USB-C connector (as shown in USB Interfaces). This communication interface is intended to be used with Alpha Data utility called avr2util. Avr2util can be run from the command line from a host PC connected to the board.

To see available options, run:

```
avr2util -?
```

To display sensor values (use -usbcom for the MicroUSB interface):

```
avr2util -usbcom \\.\COM13 display-sensors
```

To set the user-programmable clock (e.g. PROGCLK at index 1) to the factory default frequency (limited to 100 times over the lifetime of the board):

```
avr2util -usbcom \\.\COM13 setclknv-regmap 0
```

# Appendix A: Rear Connector Pinouts

## Appendix A.1: Primary XMC Connector, P5

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1: | PET_P0 | PET_N0 | 3V3 | PET_P1 | PET_N1 | VPWR |
| 2: | GND | GND | - | GND | GND | MRSTI_L |
| 3: | PET_P2 | PET_N2 | 3V3 | PET_P3 | PET_N3 | VPWR |
| 4: | GND | GND | TCK | GND | GND | MRSTO_L |
| 5: | PET_P4 | PET_N4 | 3V3 | PET_P5 | PET_N5 | VPWR |
| 6: | GND | GND | TMS | GND | GND | 12V0 |
| 7: | PET_P6 | PET_N6 | 3V3 | PET_P7 | PET_N7 | VPWR |
| 8: | GND | GND | TDI | GND | GND | M12V0 |
| 9: | - | - | - | - | - | VPWR |
| 10: | GND | GND | TDO | GND | GND | GA0 |
| 11: | PER_P0 | PER_N0 | MBIST_L | PER_P1 | PER_N1 | VPWR |
| 12: | GND | GND | GA1 | GND | GND | MPRESENT_L |
| 13: | PER_P2 | PER_N2 | 3V3_AUX | PER_P3 | PER_N3 | VPWR |
| 14: | GND | GND | GA2 | GND | GND | I2C_SDA |
| 15: | PER_P4 | PER_N4 | - | PER_P5 | PER_N5 | VPWR |
| 16: | GND | GND | MVMRO | GND | GND | MSCL |
| 17: | PER_P6 | PER_N6 | - | PER_P7 | PER_N7 | - |
| 18: | GND | GND | - | GND | GND | - |
| 19: | REFCLK0_P | REFCLK0_N | - | WAKE_L | ROOT0_L | - |

**Table 18 : Pn5 Interface**

| Signal | FPGA Pin | FPGA Bank |
|---|---|---|
| P5_PCIE_TX_PIN_P0 | AB38 | 103 |
| P5_PCIE_TX_PIN_N0 | AB39 | 103 |
| P5_PCIE_RX_PIN_P0 | AC41 | 103 |
| P5_PCIE_RX_PIN_N0 | AC42 | 103 |
| P5_PCIE_TX_PIN_P1 | AA36 | 103 |
| P5_PCIE_TX_PIN_N1 | AA37 | 103 |
| P5_PCIE_RX_PIN_P1 | AA41 | 103 |
| P5_PCIE_RX_PIN_N1 | AA42 | 103 |
| P5_PCIE_TX_PIN_P2 | Y38 | 103 |
| P5_PCIE_TX_PIN_N2 | Y39 | 103 |
| P5_PCIE_RX_PIN_P2 | W41 | 103 |
| P5_PCIE_RX_PIN_N2 | W42 | 103 |
| P5_PCIE_TX_PIN_P3 | V38 | 103 |
| P5_PCIE_TX_PIN_N3 | V39 | 103 |
| P5_PCIE_RX_PIN_P3 | U41 | 103 |
| P5_PCIE_RX_PIN_N3 | U42 | 103 |
| P5_PCIE_TX_PIN_P4 | T38 | 104 |
| P5_PCIE_TX_PIN_N4 | T39 | 104 |
| P5_PCIE_RX_PIN_P4 | R41 | 104 |
| P5_PCIE_RX_PIN_N4 | R42 | 104 |
| P5_PCIE_TX_PIN_P5 | P38 | 104 |
| P5_PCIE_TX_PIN_N5 | P39 | 104 |
| P5_PCIE_RX_PIN_P5 | N41 | 104 |
| P5_PCIE_RX_PIN_N5 | N42 | 104 |
| P5_PCIE_TX_PIN_P6 | M38 | 104 |
| P5_PCIE_TX_PIN_N6 | M39 | 104 |
| P5_PCIE_RX_PIN_P6 | L41 | 104 |
| P5_PCIE_RX_PIN_N6 | L42 | 104 |
| P5_PCIE_TX_PIN_P7 | J36 | 104 |
| P5_PCIE_TX_PIN_N7 | J37 | 104 |
| P5_PCIE_RX_PIN_P7 | K39 | 104 |
| P5_PCIE_RX_PIN_N7 | K40 | 104 |

**Table 19 : Pn5 HSSIO Pinout**

# Appendix A.2: Secondary XMC Connector, P6

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1: | PN6_TX_P0 | PN6_TX_N0 | GPIO_37 | PN6_TX_P1 | PN6_TX_N1 | GPIO_38 |
| 2: | GND | GND | GPIO_35 | GND | GND | GPIO_36 |
| 3: | PN6_TX_P2 | PN6_TX_N2 | GPIO_33 | PN6_TX_P3 | PN6_TX_N3 | GPIO_34 |
| 4: | GND | GND | GPIO_31 | GND | GND | GPIO_32 |
| 5: | PN6_TX_P4 | PN6_TX_N4 | GPIO_29 | PN6_TX_P5 | PN6_TX_N5 | GPIO_30 |
| 6: | GND | GND | GPIO_27 | GND | GND | GPIO_28 |
| 7: | PN6_TX_P6 | PN6_TX_N6 | GPIO_25 | PN6_TX_P7 | PN6_TX_N7 | GPIO_26 |
| 8: | GND | GND | GPIO_23 | GND | GND | GPIO_24 |
| 9: | PN6_TX_P8 | PN6_TX_N8 | GPIO_21 | PN6_TX_P9 | PN6_TX_N9 | GPIO_22 |
| 10: | GND | GND | GPIO_19 | GND | GND | GPIO_20 |
| 11: | PN6_RX_P0 | PN6_RX_N0 | GPIO_17 | PN6_RX_P1 | PN6_RX_N1 | GPIO_18 |
| 12: | GND | GND | GPIO_15 | GND | GND | GPIO_16 |
| 13: | PN6_RX_P2 | PN6_RX_N2 | GPIO_13 | PN6_RX_P3 | PN6_RX_N3 | GPIO_14 |
| 14: | GND | GND | GPIO_11 | GND | GND | GPIO_12 |
| 15: | PN6_RX_P4 | PN6_RX_N4 | GPIO_9 | PN6_RX_P5 | PN6_RX_N5 | GPIO_10 |
| 16: | GND | GND | GPIO_7 | GND | GND | GPIO_8 |
| 17: | PN6_RX_P6 | PN6_RX_N6 | GPIO_5 | PN6_RX_P7 | PN6_RX_N7 | GPIO_6 |
| 18: | GND | GND | GPIO_3 | GND | GND | GPIO_4 |
| 19: | N6_REFCLK_P* | PN6_REFCLK_N* | GPIO_1 | - | ROOT1_L | GPIO_2 |

**Table 20 : Pn6 Interface**

| Signal | FPGA Pin | FPGA Bank |
|---|---|---|
| PN6_TX_PIN_P0 | G1 | 203 |
| PN6_TX_PIN_N0 | F1 | 203 |
| PN6_RX_PIN_P0 | D2 | 203 |
| PN6_RX_PIN_N0 | C2 | 203 |
| PN6_TX_PIN_P1 | G3 | 203 |
| PN6_TX_PIN_N1 | F3 | 203 |
| PN6_RX_PIN_P1 | B3 | 203 |
| PN6_RX_PIN_N1 | A3 | 203 |
| PN6_TX_PIN_P2 | G5 | 203 |
| PN6_TX_PIN_N2 | F5 | 203 |
| PN6_RX_PIN_P2 | D4 | 203 |
| PN6_RX_PIN_N2 | C4 | 203 |
| PN6_TX_PIN_P3 | E6 | 203 |
| PN6_TX_PIN_N3 | D6 | 203 |
| PN6_RX_PIN_P3 | B5 | 203 |
| PN6_RX_PIN_N3 | A5 | 203 |
| PN6_TX_PIN_P4 | E8 | 204 |
| PN6_TX_PIN_N4 | D8 | 204 |
| PN6_RX_PIN_P4 | B7 | 204 |
| PN6_RX_PIN_N4 | A7 | 204 |
| PN6_TX_PIN_P5 | E10 | 204 |
| PN6_TX_PIN_N5 | D10 | 204 |
| PN6_RX_PIN_P5 | B9 | 204 |
| PN6_RX_PIN_N5 | A9 | 204 |
| PN6_TX_PIN_P6 | E12 | 204 |
| PN6_TX_PIN_N6 | D12 | 204 |
| PN6_RX_PIN_P6 | B11 | 204 |
| PN6_RX_PIN_N6 | A11 | 204 |
| PN6_TX_PIN_P7 | E14 | 204 |
| PN6_TX_PIN_N7 | D14 | 204 |
| PN6_RX_PIN_P7 | B13 | 204 |
| PN6_RX_PIN_N7 | A13 | 204 |

**Table 21 : Pn6 HSSIO Pinout**

## Appendix A.2.1: Pn6 GPIO Pin Map

| Signal | FPGA Pin | FPGA Bank | FPGA IO Standard |
|---|---|---|---|
| GPIO1 | U3 | 710 | LVCMOS15 |
| GPIO2 | Y4 | 710 | LVCMOS15 |
| GPIO3 | U4 | 710 | LVCMOS15 |
| GPIO4 | T1 | 710 | LVCMOS15 |
| GPIO5 | W3 | 710 | LVCMOS15 |
| GPIO6 | U9 | 710 | LVCMOS15 |
| GPIO7 | Y2 | 710 | LVCMOS15 |
| GPIO8 | V2 | 710 | LVCMOS15 |
| GPIO9 | V3 | 710 | LVCMOS15 |
| GPIO10 | W7 | 710 | LVCMOS15 |
| GPIO11 | N3 | 710 | LVCMOS15 |
| GPIO12 | V9 | 710 | LVCMOS15 |
| GPIO13 | W8 | 710 | LVCMOS15 |
| GPIO14 | U7 | 710 | LVCMOS15 |
| GPIO15 | V6 | 710 | LVCMOS15 |
| GPIO16 | U5 | 710 | LVCMOS15 |
| GPIO17 | U6 | 710 | LVCMOS15 |
| GPIO18 | V5 | 710 | LVCMOS15 |
| GPIO19 | W5 | 710 | LVCMOS15 |
| GPIO20 | W4 | 710 | LVCMOS15 |
| GPIO21 | V7 | 710 | LVCMOS15 |
| GPIO22 | W11 | 710 | LVCMOS15 |
| GPIO23 | U8 | 710 | LVCMOS15 |
| GPIO24 | T2 | 710 | LVCMOS15 |
| GPIO25 | W10 | 710 | LVCMOS15 |
| GPIO26 | V1 | 710 | LVCMOS15 |
| GPIO27 | R4 | 710 | LVCMOS15 |
| GPIO28 | R2 | 710 | LVCMOS15 |
| GPIO29 | P3 | 710 | LVCMOS15 |
| GPIO30 | P2 | 710 | LVCMOS15 |
| GPIO31 | N2 | 710 | LVCMOS15 |
| GPIO32 | R1 | 710 | LVCMOS15 |
| GPIO33 | W2 | 710 | LVCMOS15 |
| GPIO34 | T3 | 710 | LVCMOS15 |
| GPIO35 | P4 | 710 | LVCMOS15 |

**Table 22 : Pn6 GPIO Pin Map (continued on next page)**

| Signal | FPGA Pin | FPGA Bank | FPGA IO Standard |
|---|---|---|---|
| GPIO36 | N1 | 710 | LVCMOS15 |
| GPIO37 | U1 | 710 | LVCMOS15 |
| GPIO38 | T4 | 710 | LVCMOS15 |

**Table 22 : Pn6 GPIO Pin Map**

# Appendix A.3: PMC Connector P4

| Signal | FPGA Pin | P4 Pin | P4 Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| ETH0_MDI0_P* | - | 1 | 2 | - | ETH0_MDI2_P * |
| ETH0_MDI0_N* | - | 3 | 4 | - | ETH0_MDI2_N * |
| GND | - | 5 | 6 | - | GND |
| ETH0_MDI1_P* | - | 7 | 8 | - | ETH0_MDI3_P * |
| ETH0_MDI1_N* | - | 9 | 10 | - | ETH0_MDI3_N * |
| GND | - | 11 | 12 | - | GND |
| - | - | 13 | 14 | - | - |
| - | - | 15 | 16 | - | - |
| GND | - | 17 | 18 | - | GND |
| - | - | 19 | 20 | - | - |
| - | - | 21 | 22 | - | - |
| GND | - | 23 | 24 | - | GND |
| USB1_DM* | | 25 | 26 | - | USB2_DM* |
| USB1_DP* | | 27 | 28 | - | USB2_DP* |
| USB1_VBUS | | 29 | 30 | - | USB2_VBUS |
| GND | - | 31 | 32 | - | GND |
| - | - | 33 | 34 | - | - |
| - | - | 35 | 36 | - | - |
| - | - | 37 | 38 | - | GND |
| - | - | 39 | 40 | L18(PMC MIO42)* | COM1_RXN* |
| COM1_TXN* | L17(PMC MIO43) | 41 | 42 | L18(PMC MIO42)* | COM1_RXP* |
| COM1_TXP* | L17(PMC MIO43) | 43 | 44 | - | GND |
| COM2_TXN* | V11 | 45 | 46 | U10 | COM2_RXN* |
| COM2_TXP* | V11 | 47 | 48 | U10 | COM2_RXP* |
| GND | - | 49 | 50 | - | GND |
| CANH | F17/F16(PMC MIO48/49)* | 51 | 52 | - | - |
| CANL | F17/F16(PMC MIO48/49)* | 53 | 54 | - | - |
| GND | - | 55 | 56 | - | - |
| - | - | 57 | 58 | - | - |
| - | - | 59 | 60 | J18(PMC MIO40) | PS_GPIO3 |
| PS_GPIO1 | G19(PMC MIO36) | 61 | 62 | K18(PMC MIO41) | PS_GPIO4 |

**Table 23 : Pn4 Interface (continued on next page)**

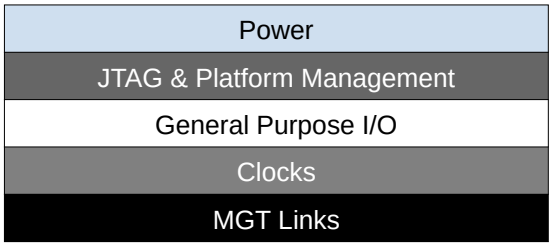
| Signal | FPGA Pin | P4 Pin | P4 Pin | FPGA Pin | Signal |
|---|---|---|---|---|---|
| PS_GPIO2 | F19(PMC MIO37) | 63 | 64 | - | GND |

**Table 23 : Pn4 Interface**

* These FPGA pins are not connect directly to the FPGA, but instead go through an on-board transceiver.

# Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



# Appendix B.1: XRM Connector CN1, Field 1

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DA_N0 | BB3 | 1 | 2 | BA9 | DA_N1 |
| DA_P0 | BA3 | 3 | 4 | BB9 | DA_P1 |
| DA_N2 | AW5 | 5 | 6 | BB5 | DA_P3 |
| DA_P2 | AV6 | 7 | 8 | BB4 | DA_N3 |
| DA_N4 | AV10 | 9 | 10 | AU3 | DA_N5 |
| DA_P4 | AV11 | 11 | 12 | AV3 | DA_P5 |
| DA_N6 | BA4 | 13 | 14 | BB10 | DA_N7 |
| DA_P6 | AY5 | 15 | 16 | BB11 | DA_P7 |
| DA_P8 | AW4 | 17 | 18 | AV2 | DA_P9 |
| DA_N8 | AY4 | 19 | 20 | AU1 | DA_N9 |
| DA_N10 | AW9 | 21 | 22 | AU4 | DA_N11 |
| DA_P10 | AW10 | 23 | 24 | AV5 | DA_P11 |
| DA_N12 | AY6 | 25 | 26 | AV1 | DA_P13 |
| DA_P12 | BA6 | 27 | 28 | AW2 | DA_N13 |
| DA_N14 | AY1 | 29 | 30 | AY2 | DA_P15 |
| DA_P14 | BA2 | 31 | 32 | AW3 | DA_N15 |
| DB_N0 | AR6 | 33 | 34 | AT10 | DB_N1 |
| DB_P0 | AT6 | 35 | 36 | AR11 | DB_P1 |
| SA_0 | AY12 | 37 | 38 | BA11 | DA_CC_P16 |
| 3V3:1 | - | 39 | 40 | AY11 | DA_CC_N16 |
| 3V3:1 | - | 41 | 42 | - | FORCE2V5_L |
| 3V3:1 | - | 43 | 44 | - | 2V5 |
| 5V0:1 | - | 45 | 46 | - | VREF |
| 5V0:1 | - | 47 | 48 | - | VccIO |
| VBATT:1 | - | 49 | 50 | - | VccIO |
| 12V0:1 | - | 51 | 52 | - | VccIO |
| 12V0:1 | - | 53 | 54 | - | M12V0 |
| PRESENCE_L | - | 55 | 56 | - | TDI |
| TCK:3 | - | 57 | 58 | - | TRST |
| TMS:3 | - | 59 | 60 | - | TDO |

**Table 24 : XRM Connector CN1, Field 1**

# Appendix B.2: XRM Connector CN1, Field 2

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DB_N2 | AU5 | 61 | 62 | AR1 | DB_N3 |
| DB_P2 | AU6 | 63 | 64 | AR2 | DB_P3 |
| DB_N4 | AP4 | 65 | 66 | AU8 | DB_N5 |
| DB_P4 | AP5 | 67 | 68 | AU9 | DB_P5 |
| DB_N6 | AT4 | 69 | 70 | AT13 | DB_N7 |
| DB_P6 | AR5 | 71 | 72 | AT14 | DB_P7 |
| DB_N8 | AR9 | 73 | 74 | AP2 | DB_P9 |
| DB_P8 | AT9 | 75 | 76 | AN1 | DB_N9 |
| DB_P10 | AM4 | 77 | 78 | AP3 | DB_N11 |
| DB_N10 | AM3 | 79 | 80 | AN3 | DB_P11 |
| DB_N12 | AU12 | 81 | 82 | AN2 | DB_P13 |
| DB_P12 | AU13 | 83 | 84 | AM1 | DB_N13 |
| DB_N14 | AT1 | 85 | 86 | AM5 | DB_N15 |
| DB_P14 | AT2 | 87 | 88 | AN5 | DB_P15 |
| DB_CC_P16:4 | AU11 | 89 | 90 | AR4 | SB_1 |
| DB_CC_N16:4 | AT11 | 91 | 92 | AJ2 | SC_0 |
| SA_1 | BA12 | 93 | 94 | AH1 | SC_1 |
| SB_0 | AT3 | 95 | 96 | AD11 | SD_0 |
| DC_CC_P16:4 | AH3 | 97 | 98 | AG4 | DC_N1 |
| DC_CC_N16:4 | AJ3 | 99 | 100 | AG5 | DC_P1 |
| DC_N0 | AK9 | 101 | 102 | AB4 | DD_CC_P16 |
| DC_P0 | AL9 | 103 | 104 | AB5 | DD_CC_N16 |
| SD_1 | AD12 | 105 | 106 | AE11 | SD_3 |
| SD_2 | AF12 | 107 | 108 | AD8 | GCLK_M2C_N |
| MGTCLK_M2-C_P:4 | L36 | 109 | 110 | AC8 | GCLK_M2C_P |
| MGTCLK_M2-C_N:4 | L37 | 111 | 112 | - | SDA |
| XRM_LVDS_C-LK_N | AY9 | 113 | 114 | - | SCL |
| XRM_LVDS_C-LK_P | AY10 | 115 | 116 | - | ALERT_N |

**Table 25 : XRM Connector CN1, Field 2 (continued on next page)**

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| MGT_C2M_P7:2 | E36 | 117 | 118 | F39 | MGT_M2C_P7 |
| MGT_C2M_N7:2 | E37 | 119 | 120 | F40 | MGT_M2C_N7 |

**Table 25 : XRM Connector CN1, Field 2**

# Appendix B.3: XRM Connector CN1, Field 3

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| DC_P2 | AK5 | 121 | 122 | AK2 | DC_P3 |
| DC_N2 | AK4 | 123 | 124 | AK1 | DC_N3 |
| DC_N4 | AJ8 | 125 | 126 | AG3 | DC_P5 |
| DC_P4 | AJ9 | 127 | 128 | AF3 | DC_N5 |
| DC_P6 | AL2 | 129 | 130 | AG1 | DC_P7 |
| DC_N6 | AL1 | 131 | 132 | AH2 | DC_N7 |
| DC_N8 | AJ10 | 133 | 134 | AF1 | DC_N9 |
| DC_P8 | AH11 | 135 | 136 | AF2 | DC_P9 |
| DC_P10 | AG6 | 137 | 138 | AH10 | DC_N11 |
| DC_N10 | AH5 | 139 | 140 | AG11 | DC_P11 |
| DC_P12 | AG9 | 141 | 142 | AJ4 | DC_N13 |
| DC_N12 | AH8 | 143 | 144 | AJ5 | DC_P13 |
| DC_N14 | AL10 | 145 | 146 | AB10 | DD_P1 |
| DC_P14 | AK11 | 147 | 148 | AB9 | DD_N1 |
| DD_P0 | AE5 | 149 | 150 | AL3 | DC_N15 |
| DD_N0 | AD4 | 151 | 152 | AL4 | DC_P15 |
| DD_P2 | AA9 | 153 | 154 | AE4 | DD_N3 |
| DD_N2 | AA8 | 155 | 156 | AF4 | DD_P3 |
| DD_N4 | AF9 | 157 | 158 | AE9 | DD_N5 |
| DD_P4 | AF10 | 159 | 160 | AE10 | DD_P5 |
| DD_P6 | AA2 | 161 | 162 | AA6 | DD_N7 |
| DD_N6 | Y1 | 163 | 164 | AB6 | DD_P7 |
| DD_N8 | AA3 | 165 | 166 | AA1 | DD_N9 |
| DD_P8 | AA4 | 167 | 168 | AB1 | DD_P9 |
| DD_N10 | AC3 | 169 | 170 | AC1 | DD_N11 |
| DD_P10 | AB3 | 171 | 172 | AC2 | DD_P11 |
| DD_N12 | AE1 | 173 | 174 | AD2 | DD_N13 |
| DD_P12 | AE2 | 175 | 176 | AD3 | DD_P13 |
| DD_N14 | AC5 | 177 | 178 | AC9 | DD_N15 |
| DD_P14 | AD5 | 179 | 180 | AC10 | DD_P15 |

**Table 26 : XRM Connector CN1, Field 3**

# Appendix B.4: XRM Connector CN2

| Signal | FPGA | Samtec | Samtec | FPGA | Signal |
|---|---|---|---|---|---|
| MGT_C2M_P0 | D34 | 1 | 2 | E41 | MGT_M2C_P0 |
| MGT_C2M_N0 | D35 | 3 | 4 | E41 | MGT_M2C_N0 |
| MGT_C2M_P1 | C36 | 5 | 6 | D39 | MGT_M2C_P1 |
| MGT_C2M_N1 | C37 | 7 | 8 | D40 | MGT_M2C_N1 |
| MGT_C2M_P4 | H34 | 9 | 10 | J41 | MGT_M2C_P4 |
| MGT_C2M_N4 | H35 | 11 | 12 | J42 | MGT_M2C_N4 |
| MGT_C2M_P5 | G36 | 13 | 14 | H39 | MGT_M2C_P5 |
| MGT_C2M_N5 | G37 | 15 | 16 | H40 | MGT_M2C_N5 |
| MGT_C2M_P2 | B34 | 17 | 18 | C41 | MGT_M2C_P2 |
| MGT_C2M_N2 | B35 | 19 | 20 | C42 | MGT_M2C_N2 |
| MGT_C2M_P3 | A36 | 21 | 22 | B39 | MGT_M2C_P3 |
| MGT_C2M_N3 | A37 | 23 | 24 | B40 | MGT_M2C_N3 |
| MGT_C2M_P6 | F34 | 25 | 26 | G41 | MGT_M2C_P6 |
| MGT_C2M_N6 | F35 | 27 | 28 | G42 | MGT_M2C_N6 |

**Table 27 : XRM Connector CN2**

# Appendix C: Full pinout table

| Signal | FPGA Pin |
|---|---|
| LPDDR4_0_CH0_CA_A[0] | AK30 |
| LPDDR4_0_CH0_CA_A[1] | AJ30 |
| LPDDR4_0_CH0_CA_A[2] | AK32 |
| LPDDR4_0_CH0_CA_A[3] | AF33 |
| LPDDR4_0_CH0_CA_A[4] | AE32 |
| LPDDR4_0_CH0_CA_A[5] | AE33 |
| LPDDR4_0_CH0_CA_B[0] | AK34 |
| LPDDR4_0_CH0_CA_B[1] | AH35 |
| LPDDR4_0_CH0_CA_B[2] | AE34 |
| LPDDR4_0_CH0_CA_B[3] | AD34 |
| LPDDR4_0_CH0_CA_B[4] | AD36 |
| LPDDR4_0_CH0_CA_B[5] | AD35 |
| LPDDR4_0_CH0_CKE_A[0] | AJ33 |
| LPDDR4_0_CH0_CKE_A[1] | AK33 |
| LPDDR4_0_CH0_CKE_B[0] | AJ34 |
| LPDDR4_0_CH0_CKE_B[1] | AK35 |
| LPDDR4_0_CH0_CK_C_A[0] | AH32 |
| LPDDR4_0_CH0_CK_T_A[0] | AG33 |
| LPDDR4_0_CH0_CK_C_B[0] | AF34 |
| LPDDR4_0_CH0_CK_T_B[0] | AF35 |
| LPDDR4_0_CH0_CS_A[0] | AF32 |
| LPDDR4_0_CH0_CS_A[1] | AJ31 |
| LPDDR4_0_CH0_CS_B[0] | AG40 |
| LPDDR4_0_CH0_CS_B[1] | AG39 |
| LPDDR4_0_CH0_DMI_A[0] | AL35 |
| LPDDR4_0_CH0_DMI_A[1] | AH38 |
| LPDDR4_0_CH0_DMI_B[0] | AK39 |
| LPDDR4_0_CH0_DMI_B[1] | AF41 |
| LPDDR4_0_CH0_DQS_C_A[0] | AM33 |
| LPDDR4_0_CH0_DQS_T_A[0] | AL32 |
| LPDDR4_0_CH0_DQS_C_A[1] | AG38 |
| LPDDR4_0_CH0_DQS_T_A[1] | AF39 |
| LPDDR4_0_CH0_DQS_C_B[0] | AN41 |
| LPDDR4_0_CH0_DQS_T_B[0] | AM40 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_0_CH0_DQS_C_B[1] | AG41 |
| LPDDR4_0_CH0_DQS_T_B[1] | AH42 |
| LPDDR4_0_CH0_DQ_A[0] | AM30 |
| LPDDR4_0_CH0_DQ_A[10] | AF38 |
| LPDDR4_0_CH0_DQ_A[11] | AE39 |
| LPDDR4_0_CH0_DQ_A[12] | AD39 |
| LPDDR4_0_CH0_DQ_A[13] | AD38 |
| LPDDR4_0_CH0_DQ_A[14] | AJ40 |
| LPDDR4_0_CH0_DQ_A[15] | AJ38 |
| LPDDR4_0_CH0_DQ_A[1] | AL31 |
| LPDDR4_0_CH0_DQ_A[2] | AN32 |
| LPDDR4_0_CH0_DQ_A[3] | AN33 |
| LPDDR4_0_CH0_DQ_A[4] | AM31 |
| LPDDR4_0_CH0_DQ_A[5] | AN31 |
| LPDDR4_0_CH0_DQ_A[6] | AM36 |
| LPDDR4_0_CH0_DQ_A[7] | AM35 |
| LPDDR4_0_CH0_DQ_A[8] | AK37 |
| LPDDR4_0_CH0_DQ_A[9] | AJ39 |
| LPDDR4_0_CH0_DQ_B[0] | AM38 |
| LPDDR4_0_CH0_DQ_B[10] | AH41 |
| LPDDR4_0_CH0_DQ_B[11] | AH40 |
| LPDDR4_0_CH0_DQ_B[12] | AK42 |
| LPDDR4_0_CH0_DQ_B[13] | AJ42 |
| LPDDR4_0_CH0_DQ_B[14] | AE40 |
| LPDDR4_0_CH0_DQ_B[15] | AE41 |
| LPDDR4_0_CH0_DQ_B[1] | AM39 |
| LPDDR4_0_CH0_DQ_B[2] | AL38 |
| LPDDR4_0_CH0_DQ_B[3] | AL39 |
| LPDDR4_0_CH0_DQ_B[4] | AL41 |
| LPDDR4_0_CH0_DQ_B[5] | AM41 |
| LPDDR4_0_CH0_DQ_B[6] | AL42 |
| LPDDR4_0_CH0_DQ_B[7] | AK41 |
| LPDDR4_0_CH0_DQ_B[8] | AE42 |
| LPDDR4_0_CH0_DQ_B[9] | AF42 |
| LPDDR4_0_CH0_RESET_N[0] | AE36 |
| LPDDR4_0_CH1_CA_A[0] | BA41 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_0_CH1_CA_A[1] | BB40 |
| LPDDR4_0_CH1_CA_A[2] | AV42 |
| LPDDR4_0_CH1_CA_A[3] | AU41 |
| LPDDR4_0_CH1_CA_A[4] | AT41 |
| LPDDR4_0_CH1_CA_A[5] | AT42 |
| LPDDR4_0_CH1_CA_B[0] | BA33 |
| LPDDR4_0_CH1_CA_B[1] | BA34 |
| LPDDR4_0_CH1_CA_B[2] | AV35 |
| LPDDR4_0_CH1_CA_B[3] | AV33 |
| LPDDR4_0_CH1_CA_B[4] | AU33 |
| LPDDR4_0_CH1_CA_B[5] | AU35 |
| LPDDR4_0_CH1_CKE_A[0] | AY41 |
| LPDDR4_0_CH1_CKE_A[1] | AW40 |
| LPDDR4_0_CH1_CKE_B[0] | AY34 |
| LPDDR4_0_CH1_CKE_B[1] | AY35 |
| LPDDR4_0_CH1_CK_C_A[0] | AW42 |
| LPDDR4_0_CH1_CK_T_A[0] | AV41 |
| LPDDR4_0_CH1_CK_C_B[0] | AW35 |
| LPDDR4_0_CH1_CK_T_B[0] | AW34 |
| LPDDR4_0_CH1_CS_A[0] | AY40 |
| LPDDR4_0_CH1_CS_A[1] | AY42 |
| LPDDR4_0_CH1_CS_B[0] | AW39 |
| LPDDR4_0_CH1_CS_B[1] | AY32 |
| LPDDR4_0_CH1_DMI_A[0] | AV38 |
| LPDDR4_0_CH1_DMI_A[1] | AT33 |
| LPDDR4_0_CH1_DMI_B[0] | AY31 |
| LPDDR4_0_CH1_DMI_B[1] | AP42 |
| LPDDR4_0_CH1_DQS_C_A[0] | AW38 |
| LPDDR4_0_CH1_DQS_T_A[0] | AY39 |
| LPDDR4_0_CH1_DQS_C_A[1] | AP33 |
| LPDDR4_0_CH1_DQS_T_A[1] | AP34 |
| LPDDR4_0_CH1_DQS_C_B[0] | AW32 |
| LPDDR4_0_CH1_DQS_T_B[0] | AW33 |
| LPDDR4_0_CH1_DQS_C_B[1] | AP40 |
| LPDDR4_0_CH1_DQS_T_B[1] | AN40 |
| LPDDR4_0_CH1_DQ_A[0] | AU39 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_0_CH1_DQ_A[10] | AT35 |
| LPDDR4_0_CH1_DQ_A[11] | AT31 |
| LPDDR4_0_CH1_DQ_A[12] | AR32 |
| LPDDR4_0_CH1_DQ_A[13] | AT34 |
| LPDDR4_0_CH1_DQ_A[14] | AP35 |
| LPDDR4_0_CH1_DQ_A[15] | AR31 |
| LPDDR4_0_CH1_DQ_A[1] | AV40 |
| LPDDR4_0_CH1_DQ_A[2] | BA38 |
| LPDDR4_0_CH1_DQ_A[3] | BA39 |
| LPDDR4_0_CH1_DQ_A[4] | BB38 |
| LPDDR4_0_CH1_DQ_A[5] | BB39 |
| LPDDR4_0_CH1_DQ_A[6] | AU40 |
| LPDDR4_0_CH1_DQ_A[7] | AU38 |
| LPDDR4_0_CH1_DQ_A[8] | AP31 |
| LPDDR4_0_CH1_DQ_A[9] | AR35 |
| LPDDR4_0_CH1_DQ_B[0] | AU31 |
| LPDDR4_0_CH1_DQ_B[10] | AR42 |
| LPDDR4_0_CH1_DQ_B[11] | AP39 |
| LPDDR4_0_CH1_DQ_B[12] | AP38 |
| LPDDR4_0_CH1_DQ_B[13] | AR40 |
| LPDDR4_0_CH1_DQ_B[14] | AR39 |
| LPDDR4_0_CH1_DQ_B[15] | AN38 |
| LPDDR4_0_CH1_DQ_B[1] | BB31 |
| LPDDR4_0_CH1_DQ_B[2] | AV31 |
| LPDDR4_0_CH1_DQ_B[3] | AV32 |
| LPDDR4_0_CH1_DQ_B[4] | BA31 |
| LPDDR4_0_CH1_DQ_B[5] | BB33 |
| LPDDR4_0_CH1_DQ_B[6] | BA32 |
| LPDDR4_0_CH1_DQ_B[7] | AU32 |
| LPDDR4_0_CH1_DQ_B[8] | AR41 |
| LPDDR4_0_CH1_DQ_B[9] | AT39 |
| LPDDR4_0_CH1_RESET_N[0] | AD37 |
| LPDDR4_1_CH0_CA_A[0] | AJ25 |
| LPDDR4_1_CH0_CA_A[1] | AH25 |
| LPDDR4_1_CH0_CA_A[2] | AL26 |
| LPDDR4_1_CH0_CA_A[3] | AL28 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_1_CH0_CA_A[4] | AJ28 |
| LPDDR4_1_CH0_CA_A[5] | AK29 |
| LPDDR4_1_CH0_CA_B[0] | AM25 |
| LPDDR4_1_CH0_CA_B[1] | AP25 |
| LPDDR4_1_CH0_CA_B[2] | AN29 |
| LPDDR4_1_CH0_CA_B[3] | AM28 |
| LPDDR4_1_CH0_CA_B[4] | AP29 |
| LPDDR4_1_CH0_CA_B[5] | AP30 |
| LPDDR4_1_CH0_CKE_A[0] | AK26 |
| LPDDR4_1_CH0_CKE_A[1] | AL25 |
| LPDDR4_1_CH0_CKE_B[0] | AP26 |
| LPDDR4_1_CH0_CKE_B[1] | AN25 |
| LPDDR4_1_CH0_CK_C_A[0] | AJ27 |
| LPDDR4_1_CH0_CK_T_A[0] | AH26 |
| LPDDR4_1_CH0_CK_C_B[0] | AP27 |
| LPDDR4_1_CH0_CK_T_B[0] | AN28 |
| LPDDR4_1_CH0_CS_A[0] | AL29 |
| LPDDR4_1_CH0_CS_A[1] | AK27 |
| LPDDR4_1_CH0_CS_B[0] | BB28 |
| LPDDR4_1_CH0_CS_B[1] | AU28 |
| LPDDR4_1_CH0_DMI_A[0] | AN24 |
| LPDDR4_1_CH0_DMI_A[1] | AU27 |
| LPDDR4_1_CH0_DMI_B[0] | AW25 |
| LPDDR4_1_CH0_DMI_B[1] | BA29 |
| LPDDR4_1_CH0_DQS_C_A[0] | AL23 |
| LPDDR4_1_CH0_DQS_T_A[0] | AK24 |
| LPDDR4_1_CH0_DQS_C_A[1] | AW28 |
| LPDDR4_1_CH0_DQS_T_A[1] | AV28 |
| LPDDR4_1_CH0_DQS_C_B[0] | BB23 |
| LPDDR4_1_CH0_DQS_T_B[0] | BA23 |
| LPDDR4_1_CH0_DQS_C_B[1] | BA28 |
| LPDDR4_1_CH0_DQS_T_B[1] | AY27 |
| LPDDR4_1_CH0_DQ_A[0] | AJ24 |
| LPDDR4_1_CH0_DQ_A[1] | AK23 |
| LPDDR4_1_CH0_DQ_A[2] | AR23 |
| LPDDR4_1_CH0_DQ_A[3] | AR24 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_1_CH0_DQ_A[4] | AN23 |
| LPDDR4_1_CH0_DQ_A[5] | AJ22 |
| LPDDR4_1_CH0_DQ_A[6] | AP23 |
| LPDDR4_1_CH0_DQ_A[7] | AH22 |
| LPDDR4_1_CH0_DQ_A[8] | AV30 |
| LPDDR4_1_CH0_DQ_A[9] | AW30 |
| LPDDR4_1_CH0_DQ_A[10] | AV26 |
| LPDDR4_1_CH0_DQ_A[11] | AW29 |
| LPDDR4_1_CH0_DQ_A[12] | AW27 |
| LPDDR4_1_CH0_DQ_A[13] | AV27 |
| LPDDR4_1_CH0_DQ_A[14] | AU25 |
| LPDDR4_1_CH0_DQ_A[15] | AU29 |
| LPDDR4_1_CH0_DQ_B[0] | AY24 |
| LPDDR4_1_CH0_DQ_B[1] | BB25 |
| LPDDR4_1_CH0_DQ_B[2] | BB24 |
| LPDDR4_1_CH0_DQ_B[3] | AW24 |
| LPDDR4_1_CH0_DQ_B[4] | AU24 |
| LPDDR4_1_CH0_DQ_B[5] | AV25 |
| LPDDR4_1_CH0_DQ_B[6] | BA24 |
| LPDDR4_1_CH0_DQ_B[7] | AW23 |
| LPDDR4_1_CH0_DQ_B[8] | AY29 |
| LPDDR4_1_CH0_DQ_B[9] | BA27 |
| LPDDR4_1_CH0_DQ_B[10] | AY26 |
| LPDDR4_1_CH0_DQ_B[11] | BA26 |
| LPDDR4_1_CH0_DQ_B[12] | BB26 |
| LPDDR4_1_CH0_DQ_B[13] | BB29 |
| LPDDR4_1_CH0_DQ_B[14] | BB30 |
| LPDDR4_1_CH0_DQ_B[15] | AY30 |
| LPDDR4_1_CH0_RESET_N[0] | AR29 |
| LPDDR4_1_CH1_CA_A[0] | BA16 |
| LPDDR4_1_CH1_CA_A[1] | AY15 |
| LPDDR4_1_CH1_CA_A[2] | BB19 |
| LPDDR4_1_CH1_CA_A[3] | BA18 |
| LPDDR4_1_CH1_CA_A[4] | AY19 |
| LPDDR4_1_CH1_CA_A[5] | BA19 |
| LPDDR4_1_CH1_CA_B[0] | AN16 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_1_CH1_CA_B[1] | AP15 |
| LPDDR4_1_CH1_CA_B[2] | AN19 |
| LPDDR4_1_CH1_CA_B[3] | AM19 |
| LPDDR4_1_CH1_CA_B[4] | AL19 |
| LPDDR4_1_CH1_CA_B[5] | AM18 |
| LPDDR4_1_CH1_CKE_A[0] | BB16 |
| LPDDR4_1_CH1_CKE_A[1] | AY17 |
| LPDDR4_1_CH1_CKE_B[0] | AN17 |
| LPDDR4_1_CH1_CKE_B[1] | AM16 |
| LPDDR4_1_CH1_CK_C_A[0] | BA17 |
| LPDDR4_1_CH1_CK_T_A[0] | BB18 |
| LPDDR4_1_CH1_CK_C_B[0] | AP17 |
| LPDDR4_1_CH1_CK_T_B[0] | AP18 |
| LPDDR4_1_CH1_CS_A[0] | AY16 |
| LPDDR4_1_CH1_CS_A[1] | BB15 |
| LPDDR4_1_CH1_CS_B[0] | AV17 |
| LPDDR4_1_CH1_CS_B[1] | AK17 |
| LPDDR4_1_CH1_DMI_A[0] | AW17 |
| LPDDR4_1_CH1_DMI_A[1] | AM22 |
| LPDDR4_1_CH1_DMI_B[0] | AL16 |
| LPDDR4_1_CH1_DMI_B[1] | AY21 |
| LPDDR4_1_CH1_DQS_C_A[0] | AU17 |
| LPDDR4_1_CH1_DQS_T_A[0] | AV16 |
| LPDDR4_1_CH1_DQS_C_A[1] | AP22 |
| LPDDR4_1_CH1_DQS_T_A[1] | AN21 |
| LPDDR4_1_CH1_DQS_C_B[0] | AL17 |
| LPDDR4_1_CH1_DQS_T_B[0] | AK18 |
| LPDDR4_1_CH1_DQS_C_B[1] | AW20 |
| LPDDR4_1_CH1_DQS_T_B[1] | AY20 |
| LPDDR4_1_CH1_DQ_A[0] | AU15 |
| LPDDR4_1_CH1_DQ_A[10] | AP21 |
| LPDDR4_1_CH1_DQ_A[11] | AH20 |
| LPDDR4_1_CH1_DQ_A[12] | AN20 |
| LPDDR4_1_CH1_DQ_A[13] | AJ21 |
| LPDDR4_1_CH1_DQ_A[14] | AL20 |
| LPDDR4_1_CH1_DQ_A[15] | AK20 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| LPDDR4_1_CH1_DQ_A[1] | AV15 |
| LPDDR4_1_CH1_DQ_A[2] | AU16 |
| LPDDR4_1_CH1_DQ_A[3] | AU19 |
| LPDDR4_1_CH1_DQ_A[4] | AW15 |
| LPDDR4_1_CH1_DQ_A[5] | AW18 |
| LPDDR4_1_CH1_DQ_A[6] | AW19 |
| LPDDR4_1_CH1_DQ_A[7] | AV18 |
| LPDDR4_1_CH1_DQ_A[8] | AL22 |
| LPDDR4_1_CH1_DQ_A[9] | AK21 |
| LPDDR4_1_CH1_DQ_B[0] | AJ15 |
| LPDDR4_1_CH1_DQ_B[1] | AH16 |
| LPDDR4_1_CH1_DQ_B[2] | AH17 |
| LPDDR4_1_CH1_DQ_B[3] | AJ19 |
| LPDDR4_1_CH1_DQ_B[4] | AK15 |
| LPDDR4_1_CH1_DQ_B[5] | AJ18 |
| LPDDR4_1_CH1_DQ_B[6] | AJ16 |
| LPDDR4_1_CH1_DQ_B[7] | AH19 |
| LPDDR4_1_CH1_DQ_B[8] | BB21 |
| LPDDR4_1_CH1_DQ_B[9] | BA21 |
| LPDDR4_1_CH1_DQ_B[10] | BB20 |
| LPDDR4_1_CH1_DQ_B[11] | AW22 |
| LPDDR4_1_CH1_DQ_B[12] | AV20 |
| LPDDR4_1_CH1_DQ_B[13] | AV21 |
| LPDDR4_1_CH1_DQ_B[14] | AV22 |
| LPDDR4_1_CH1_DQ_B[15] | BA22 |
| LPDDR4_1_CH1_RESET_N[0] | AT30 |
| P5_PCIE_TX_P0 | AB38 |
| P5_PCIE_TX_N0 | AB39 |
| P5_PCIE_TX_P1 | AA36 |
| P5_PCIE_TX_N1 | AA37 |
| P5_PCIE_TX_P2 | Y38 |
| P5_PCIE_TX_N2 | Y39 |
| P5_PCIE_TX_P3 | V38 |
| P5_PCIE_TX_N3 | V39 |
| P5_PCIE_TX_P4 | T38 |
| P5_PCIE_TX_N4 | T39 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| P5_PCIE_TX_P5 | P38 |
| P5_PCIE_TX_N5 | P39 |
| P5_PCIE_TX_P6 | M38 |
| P5_PCIE_TX_N6 | M39 |
| P5_PCIE_TX_P7 | J36 |
| P5_PCIE_TX_N7 | J37 |
| P5_PCIE_RX_P0 | AC41 |
| P5_PCIE_RX_N0 | AC42 |
| P5_PCIE_RX_P1 | AA41 |
| P5_PCIE_RX_N1 | AA42 |
| P5_PCIE_RX_P2 | W41 |
| P5_PCIE_RX_N2 | W42 |
| P5_PCIE_RX_P3 | U41 |
| P5_PCIE_RX_N3 | U42 |
| P5_PCIE_RX_P4 | R41 |
| P5_PCIE_RX_N4 | R42 |
| P5_PCIE_RX_P5 | N41 |
| P5_PCIE_RX_N5 | N42 |
| P5_PCIE_RX_P6 | L41 |
| P5_PCIE_RX_N6 | L42 |
| P5_PCIE_RX_P7 | K39 |
| P5_PCIE_RX_N7 | K40 |
| PN6_TX_P0 | G1 |
| PN6_TX_N0 | F1 |
| PN6_TX_P1 | G3 |
| PN6_TX_N1 | F3 |
| PN6_TX_P2 | G5 |
| PN6_TX_N2 | F5 |
| PN6_TX_P3 | E6 |
| PN6_TX_N3 | D6 |
| PN6_TX_P4 | E8 |
| PN6_TX_N4 | D8 |
| PN6_TX_P5 | E10 |
| PN6_TX_N5 | D10 |
| PN6_TX_P6 | E12 |
| PN6_TX_N6 | D12 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| PN6_TX_P7 | E14 |
| PN6_TX_N7 | D14 |
| PN6_RX_P0 | D2 |
| PN6_RX_N0 | C2 |
| PN6_RX_P1 | B3 |
| PN6_RX_N1 | A3 |
| PN6_RX_P2 | D4 |
| PN6_RX_N2 | C4 |
| PN6_RX_P3 | B5 |
| PN6_RX_N3 | A5 |
| PN6_RX_P4 | B7 |
| PN6_RX_N4 | A7 |
| PN6_RX_P5 | B9 |
| PN6_RX_N5 | A9 |
| PN6_RX_P6 | B11 |
| PN6_RX_N6 | A11 |
| PN6_RX_P7 | B13 |
| PN6_RX_N7 | A13 |
| GPIO1 | U3 |
| GPIO2 | Y4 |
| GPIO3 | U4 |
| GPIO4 | T1 |
| GPIO5 | W3 |
| GPIO6 | U9 |
| GPIO7 | Y2 |
| GPIO8 | V2 |
| GPIO9 | V3 |
| GPIO10 | W7 |
| GPIO11 | N3 |
| GPIO12 | V9 |
| GPIO13 | W8 |
| GPIO14 | U7 |
| GPIO15 | V6 |
| GPIO16 | U5 |
| GPIO17 | U6 |
| GPIO18 | V5 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| GPIO19 | W5 |
| GPIO20 | W4 |
| GPIO21 | V7 |
| GPIO22 | W11 |
| GPIO23 | U8 |
| GPIO24 | T2 |
| GPIO25 | W10 |
| GPIO26 | V1 |
| GPIO27 | R4 |
| GPIO28 | R2 |
| GPIO29 | P3 |
| GPIO30 | P2 |
| GPIO31 | N2 |
| GPIO32 | R1 |
| GPIO33 | W2 |
| GPIO34 | T3 |
| GPIO35 | P4 |
| GPIO36 | N1 |
| GPIO37 | U1 |
| GPIO38 | T4 |
| AVR_MON_B2U_1V5 | R5 |
| AVR_MON_CLK_1V5 | R7 |
| AVR_MON_U2B_1V5 | P5 |
| CAN_RX_1V8 | F16 |
| CAN_TX_1V8 | F17 |
| ETH0_MDC | F28 |
| ETH0_MDIO | G28 |
| ETH0_RXD0 | G31 |
| ETH0_RXD1 | F31 |
| ETH0_RXD2 | E31 |
| ETH0_RXD3 | C31 |
| ETH0_RX_CLK | H32 |
| ETH0_RX_CTRL | B31 |
| ETH0_TXD0 | B32 |
| ETH0_TXD1 | C32 |
| ETH0_TXD2 | D32 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| ETH0_TXD3 | E32 |
| ETH0_TX_CTRL | G32 |
| FPGA_USER_SWITCH | R6 |
| USER_LED0_1V5_L | Y13 |
| USER_LED1_1V5_L | Y12 |
| MBIST_L_1V5 | W13 |
| MVMRO_1V5_N | K16 |
| PCIE0_MRSTI_1V8_L | F18 |
| PCIE0_MRSTI_1V8_L | G18 |
| PCIE_MRSTI_L_1V5 | Y10 |
| PCIE_MRSTO_L_1V5 | W9 |
| PCIE_ROOT0_L_1V5 | U13 |
| PCIE_WAKE_L_1V5 | U12 |
| PMC_SYSMON_SCL | G29 |
| PMC_SYSMON_SDA | F29 |
| PROGCLK3_P | AJ7 |
| PROGCLK3_N | AH6 |
| PROGCLK3_P | N36 |
| PROGCLK3_N | N37 |
| REFCLK100M2_P | R36 |
| REFCLK100M2_N | R37 |
| REFCLK_300M0_P | AF36 |
| REFCLK_300M0_N | AF37 |
| REFCLK_300M1_P | AR28 |
| REFCLK_300M1_N | AT29 |
| REFCLK_300M2_P | AC7 |
| REFCLK_300M2_N | AC6 |
| PS_SCL | K17 |
| PS_SDA | J17 |
| PS_SDA | P7 |
| PS_SCL | T6 |
| QSPI0_IO0 | H30 |
| QSPI0_IO1 | K32 |
| QSPI0_IO2 | K31 |
| QSPI0_IO3 | H31 |
| QSPI1_IO0 | L29 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| QSPI1_IO1 | J29 |
| QSPI1_IO2 | H29 |
| QSPI1_IO3 | J28 |
| QSPI_CS0_B | J30 |
| QSPI_CS1_B | L30 |
| ROOT1_L_1V1 | AP37 |
| SDIO_CMD_LS | H20 |
| SDIO_DAT0_LS | J20 |
| SDIO_DAT1_LS | K20 |
| SDIO_DAT2_LS | L20 |
| SDIO_DAT3_LS | L19 |
| SDIO_SEL_LS | J19 |
| UART0_485_EN_1V5 | J8 |
| UART0_TE485_EN_1V5 | K9 |
| UART1_485_EN_1V5 | L8 |
| UART0_RX | L18 |
| UART0_TX | L17 |
| UART1_TX | H17 |
| UART1_RX | G17 |
| UART1_RX_1V5 | U10 |
| UART1_TE485_EN_1V5 | L9 |
| UART1_TX_1V5 | V11 |
| USB0_CLK | G26 |
| USB0_D<0> | K27 |
| USB0_D<1> | J27 |
| USB0_D<2> | H27 |
| USB0_D<3> | G27 |
| USB0_D<4> | H26 |
| USB0_D<5> | K26 |
| USB0_D<6> | L26 |
| USB0_D<7> | L25 |
| USB0_DIR | K25 |
| USB0_NXT | H25 |
| USB0_RESET | L28 |
| USB0_STP | J25 |
| XRM_CLKIN_N | AC8 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| XRM_CLKIN_P | AD8 |
| XRM_DA_CC_N16 | AY11 |
| XRM_DA_CC_P16 | BA11 |
| XRM_DA_N0 | BA3 |
| XRM_DA_P0 | BB3 |
| XRM_DA_N1 | BA9 |
| XRM_DA_P1 | BB9 |
| XRM_DA_N2 | AW5 |
| XRM_DA_P2 | AV6 |
| XRM_DA_N3 | BB4 |
| XRM_DA_P3 | BB5 |
| XRM_DA_N4 | AV10 |
| XRM_DA_P4 | AV11 |
| XRM_DA_N5 | AU3 |
| XRM_DA_P5 | AV3 |
| XRM_DA_N6 | BA4 |
| XRM_DA_P6 | AY5 |
| XRM_DA_N7 | BB10 |
| XRM_DA_P7 | BB11 |
| XRM_DA_N8 | AY4 |
| XRM_DA_P8 | AW4 |
| XRM_DA_N9 | AU1 |
| XRM_DA_P9 | AV2 |
| XRM_DA_N10 | AW9 |
| XRM_DA_P10 | AW10 |
| XRM_DA_N11 | AU4 |
| XRM_DA_P11 | AV5 |
| XRM_DA_N12 | AY6 |
| XRM_DA_P12 | BA6 |
| XRM_DA_N13 | AW2 |
| XRM_DA_P13 | AV1 |
| XRM_DA_N14 | AY1 |
| XRM_DA_P14 | BA2 |
| XRM_DA_N15 | AW3 |
| XRM_DA_P15 | AY2 |
| XRM_DB_CC_P16 | AU11 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| XRM_DB_CC_N16 | AT11 |
| XRM_DB_N0 | AR6 |
| XRM_DB_P0 | AT6 |
| XRM_DB_N1 | AT10 |
| XRM_DB_P1 | AR11 |
| XRM_DB_N2 | AU5 |
| XRM_DB_P2 | AU6 |
| XRM_DB_N3 | AR1 |
| XRM_DB_P3 | AR2 |
| XRM_DB_N4 | AP4 |
| XRM_DB_P4 | AP5 |
| XRM_DB_N5 | AU8 |
| XRM_DB_P5 | AU9 |
| XRM_DB_N6 | AT4 |
| XRM_DB_P6 | AR5 |
| XRM_DB_N7 | AT13 |
| XRM_DB_P7 | AT14 |
| XRM_DB_N8 | AR9 |
| XRM_DB_P8 | AT9 |
| XRM_DB_N9 | AN1 |
| XRM_DB_P9 | AP2 |
| XRM_DB_N10 | AM3 |
| XRM_DB_P10 | AM4 |
| XRM_DB_N11 | AP3 |
| XRM_DB_P11 | AN3 |
| XRM_DB_N12 | AU12 |
| XRM_DB_P12 | AU13 |
| XRM_DB_N13 | AM1 |
| XRM_DB_P13 | AN2 |
| XRM_DB_N14 | AT1 |
| XRM_DB_P14 | AT2 |
| XRM_DB_N15 | AM5 |
| XRM_DB_P15 | AN5 |
| XRM_DC_CC_P16 | AH3 |
| XRM_DC_CC_N16 | AJ3 |
| XRM_DC_P0 | AL9 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| XRM_DC_N0 | AK9 |
| XRM_DC_P1 | AG5 |
| XRM_DC_N1 | AG4 |
| XRM_DC_P2 | AK5 |
| XRM_DC_N2 | AK4 |
| XRM_DC_P3 | AK2 |
| XRM_DC_N3 | AK1 |
| XRM_DC_P4 | AJ9 |
| XRM_DC_N4 | AJ8 |
| XRM_DC_P5 | AG3 |
| XRM_DC_N5 | AF3 |
| XRM_DC_P6 | AL2 |
| XRM_DC_N6 | AL1 |
| XRM_DC_P7 | AG1 |
| XRM_DC_N7 | AH2 |
| XRM_DC_P8 | AH11 |
| XRM_DC_N8 | AJ10 |
| XRM_DC_P9 | AF2 |
| XRM_DC_N9 | AF1 |
| XRM_DC_P10 | AG6 |
| XRM_DC_N10 | AH5 |
| XRM_DC_P11 | AG11 |
| XRM_DC_N11 | AH10 |
| XRM_DC_P12 | AG9 |
| XRM_DC_N12 | AH8 |
| XRM_DC_P13 | AJ5 |
| XRM_DC_N13 | AJ4 |
| XRM_DC_P14 | AK11 |
| XRM_DC_N14 | AL10 |
| XRM_DC_P15 | AL4 |
| XRM_DC_N15 | AL3 |
| XRM_DD_CC_P16 | AB4 |
| XRM_DD_CC_N16 | AB5 |
| XRM_DD_P0 | AE5 |
| XRM_DD_N0 | AD4 |
| XRM_DD_P1 | AB10 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| XRM_DD_N1 | AB9 |
| XRM_DD_P2 | AA9 |
| XRM_DD_N2 | AA8 |
| XRM_DD_P3 | AF4 |
| XRM_DD_N3 | AE4 |
| XRM_DD_P4 | AF10 |
| XRM_DD_N4 | AF9 |
| XRM_DD_P5 | AE10 |
| XRM_DD_N5 | AE9 |
| XRM_DD_P6 | AA2 |
| XRM_DD_N6 | Y1 |
| XRM_DD_P7 | AB6 |
| XRM_DD_N7 | AA6 |
| XRM_DD_P8 | AA4 |
| XRM_DD_N8 | AA3 |
| XRM_DD_P9 | AB1 |
| XRM_DD_N9 | AA1 |
| XRM_DD_P10 | AB3 |
| XRM_DD_N10 | AC3 |
| XRM_DD_P11 | AC2 |
| XRM_DD_N11 | AC1 |
| XRM_DD_P12 | AE2 |
| XRM_DD_N12 | AE1 |
| XRM_DD_P13 | AD3 |
| XRM_DD_N13 | AD2 |
| XRM_DD_P14 | AD5 |
| XRM_DD_N14 | AC5 |
| XRM_DD_P15 | AC10 |
| XRM_DD_N15 | AC9 |
| XRM_SA_0 | AY12 |
| XRM_SA_1 | BA12 |
| XRM_SB_0 | AT3 |
| XRM_SB_1 | AR4 |
| XRM_SCL_TEST | L13 |
| XRM_SC_0 | AJ2 |
| XRM_SC_1 | AH1 |

**Table 28 : Full Pin Map (continued on next page)**

| Signal | FPGA Pin |
|---|---|
| XRM_SDA_TEST | K13 |
| XRM_SD_0 | AD11 |
| XRM_SD_1 | AD12 |
| XRM_SD_2 | AF12 |
| XRM_SD_3 | AE11 |
| XRM_MGTCLK_M2C_N | L37 |
| XRM_MGTCLK_M2C_P | L36 |
| XRM_PECL_N | AY9 |
| XRM_PECL_P | AY10 |
| XRM_PRESENCE_L_1V5 | J9 |

**Table 28 : Full Pin Map**

# Revision History

| Date | Revision | Nature of Change | Section |
|---|---|---|---|
| 13 Nov 2024 | 0.1 | Initial Draft | N/A |
| 30 Jan 2025 | 1.0 | Initial Release | N/A |

Address: Suite L4A, 160 Dundee Street,
Edinburgh, EH11 1DQ, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 10822 West Toller Drive, Suite 250
Littleton, CO 80127
Telephone: (303) 954 8768
Fax: (866) 820 9956 - toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com